Nokia Customer Care
2115i/2116/2116i (RH-66)
Mobile Terminals

Baseband Description and Troubleshooting

Contents

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Introduction

The mobile terminal uses a CDMA tri-mode engine (AMPS/800/1900) with a DCT4 baseband consisting of three ASICs:

- Universal Energy Management cost reduction (UEMC)
- Universal Phone Processor (UPP) - UPP8Mv4.2
- 8MB flash memory with 1 MB of RAM memory

The baseband architecture supports a power-saving function called sleep mode. Sleep mode shuts off the voltage-controlled temperature-compensated crystal oscillator (VCTCXO), which is used as the system clock source for both the RF and the baseband. During sleep mode, the system runs from a 32 kHz crystal and all the RF regulators (VR1A, VR1B, VR2—VR7) are off. The sleep time is determined by network parameters. Sleep mode is entered when both the Master Control Unit (MCU) and the Digital Signal Processor (DSP) are in standby mode and the normal VCTCXO clock is switched off. The mobile terminal is awakened by a timer running from this 32 kHz clock supply. The period of the sleep/wake up cycle (slotted cycle) is 1.28N seconds, where N= 0, 1, 2, depending on the slot cycle index.

The mobile terminal supports standard Nokia 2-wire and 3-wire chargers (ACP-x and LCH-x). However, the 3-wire chargers are treated as 2-wire chargers. The PWM control signal for controlling the 3-wire charger is ignored. The UEMC and energy management software control charging.

A BL-6C (1070 mAh) lithium-ion battery is used as the main power source.

Baseband and RF Architecture

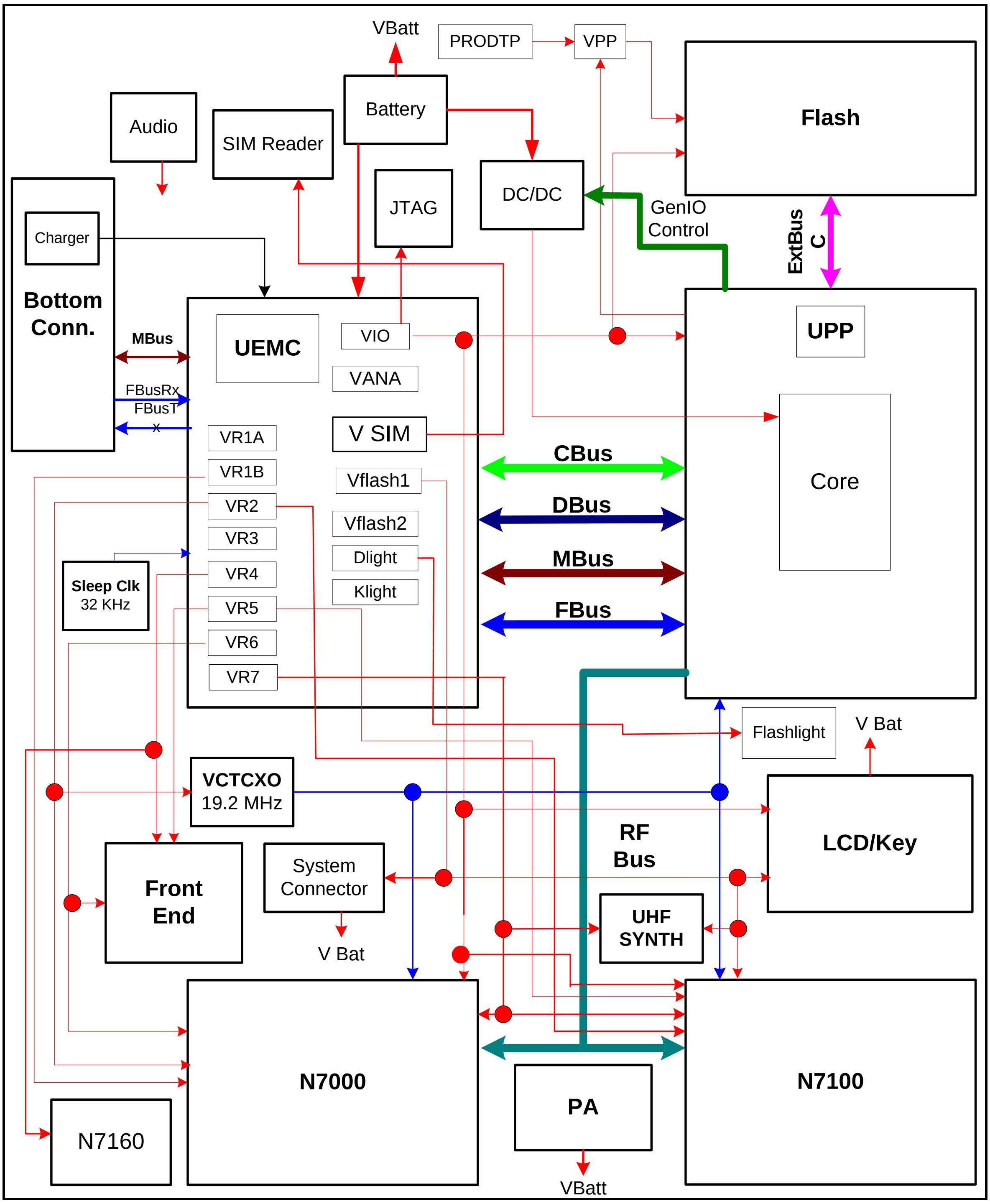


Figure 1: Power distribution

Power Up and Reset

The UEMC ASIC controls the power up and reset. The baseband can power up in the following ways:

- Pressing the Power button, which means grounding the PWRONX pin of the UEMC
- Connecting the charger to the charger input
- Initiating the real-time clock (RTC) alarm (when the RTC logic has been programmed to give an alarm)

After receiving one of the above signals, the UEMC counts a 20 ms delay and then enters reset mode. The watchdog starts, and if the battery voltage is greater than Vcoff+, a 200 ms delay starts to allow references (etc.) to settle. After this delay elapses, the VFLASH1 regulator enables. Then, 500 us later, the VR3, VANA, VIO, and VCORE enable. The Power Up Reset (PURX) line holds low for 20 ms and is sent to the UPP. Resets are generated for the MCU and the DSP. During this reset phase, the UEMC forces the VCTCXO regulator on regardless of the status of the sleep control input signal to the UEMC.

The FLSRSTx from the UPP is used to reset the flash during power up and to put the flash in power down during sleep mode. All baseband regulators are switched on when the UEMC is powered on. The UEMC internal watchdogs run during the UEMC reset state, with the longest watchdog time selected. If the watchdog expires, the UEMC returns to the power-off state. The UEMC watchdogs are internally acknowledged at the rising edge of the PURX signal to always give the same watchdog response time to the MCU.

Figure 2 and Figure 3 represent the UEMC start-up sequence from reset to power-on mode.

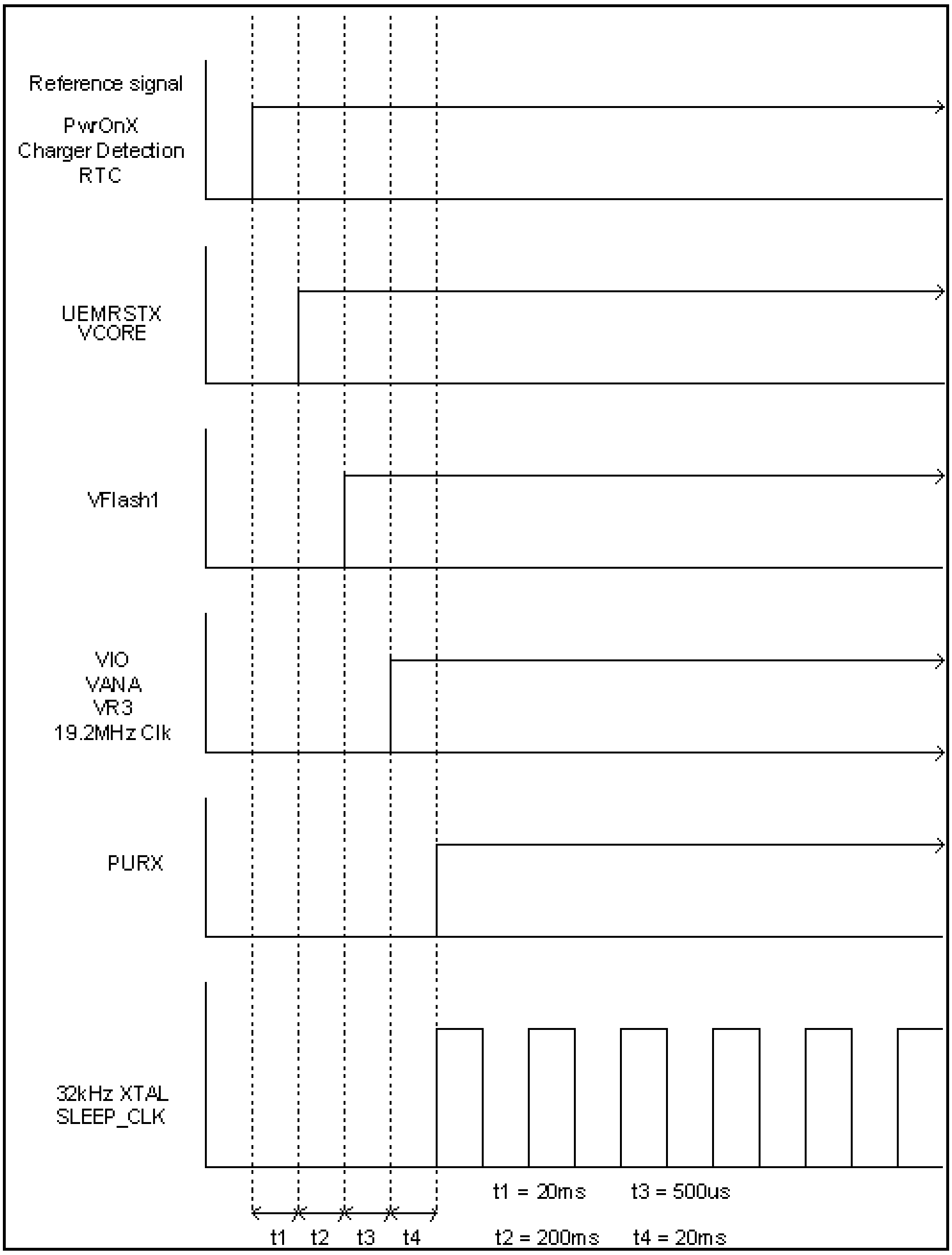


Figure 2: Power-on sequence and timing

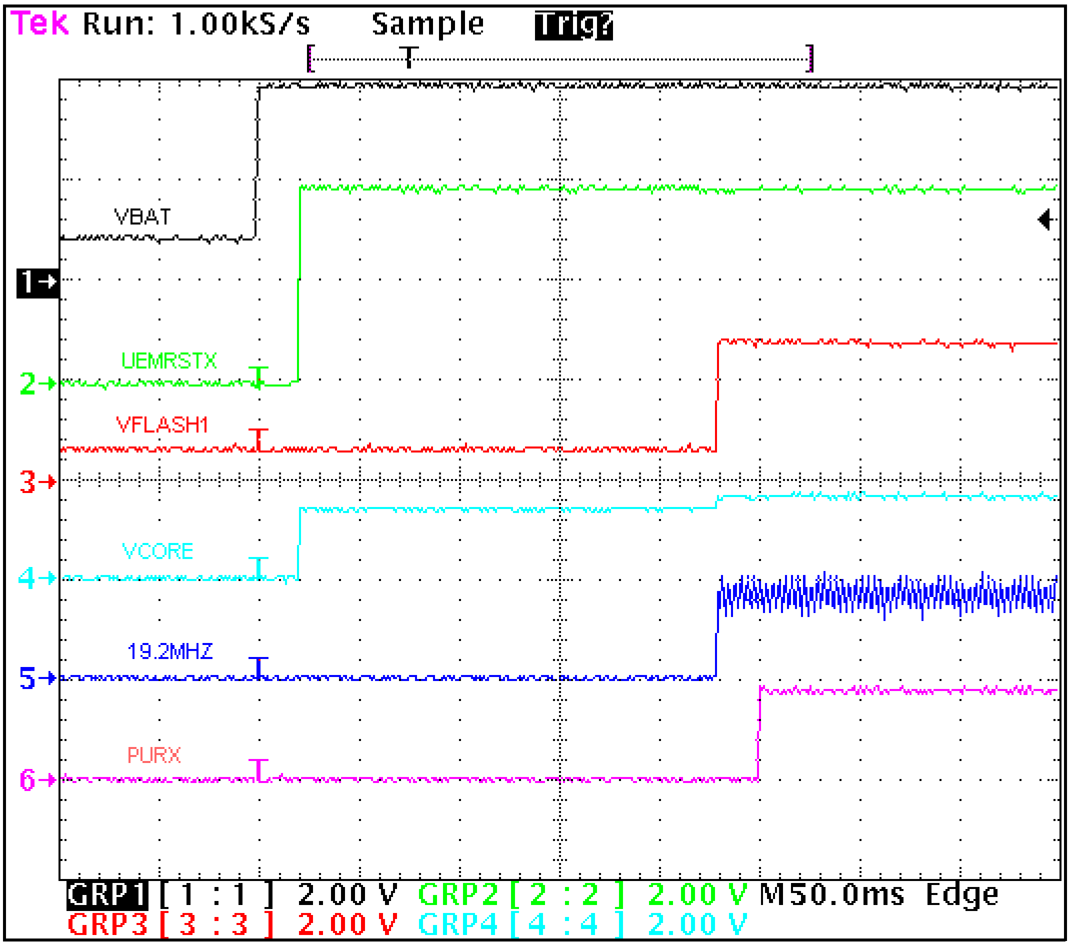


Figure 3: Measured power-on sequence and timing

Power Up

The mobile terminal can power up using the power key, a charger, or an RTC alarm.

Power Key

When the power key is pressed, the UEMC enters the power-up sequence. Pressing the power key causes the PWRONX pin on the UEMC to ground. The UEMC PWRONX signal is not part of the keypad matrix. The power key is only connected to the UEMC. This means that when pressing the power key an interrupt is generated to the UPP that starts the MCU. The MCU then reads the UEMC interrupt register and notices that it is a PWRONX interrupt. The MCU reads the status of the PWRONX signal using the UEMC control bus (CBUS). If the PWRONX signal stays low for a certain time the MCU accepts this as a valid power-on state and continues with the software baseband initialization. If the power key does not indicate a valid power-on situation, the MCU powers off the baseband.

Charger

Charging is controlled by start-up charging circuitry in order to detect and start charging in cases where the main battery is empty and the UEMC has no supply (NO_SUPPLY or BACKUP mode).

Charging is controlled by START_UP charge circuitry when it detects the VBAT level to be below the master reset threshold (V_{MSTR-}). Connecting a charger forces the VCHAR input to rise above the charger detection threshold (VCH_{DET+}), and by detection start-up charging initiates. The UEMC generates 100 mA of constant output current from the connected charger's output voltage. The battery's voltage rises at it charges, and when the VBAT voltage level is detected to be higher than the master reset threshold limit (V_{MSTR+}), the START_UP charge is terminated.

The charge control (CHACON) monitors the VBAT voltage level. A MSTRX='1' output reset signal (internal to the UEMC) is given to the UEMC's reset block when the VBAT is greater than the V_{MSTR+} and the UEMC enters into the reset sequence.

If the VBAT is detected to fall below V_{MSTR} during start-up charging, charging is cancelled. Charging restarts if a new rising edge on the VCHAR input is detected (VCHAR rising above VCH_{DET+}).

RTC Alarm

If the mobile terminal is in power-off mode when the RTC alarm begins, the wake-up procedure occurs. After the baseband is powered on, an interrupt is given to the MCU. When an RTC alarm occurs during active mode, the interrupt is generated to the MCU.

Power Off

The baseband switches to power-off mode if any of following occurs:

- Power key is pressed
- Battery voltage is too low (VBATT < 3.2 V)
- Watchdog timer register expires

The UEMC controls the power-down procedure.

Power Consumption and Operation Modes

Power-off Mode

In power-off mode, power (VBAT) is supplied to the UEMC, vibra, LED, PA, and PA drivers. During this mode, the current consumption is approximately 35 uA.

Sleep Mode

In sleep mode, both processors (MCU and DSP) are in stand-by. The mobile terminal enters sleep mode only when both processors make the request. When the UEMC detects as low SLEEPX signal, the mobile terminal enters sleep mode. The VIO and VFLASH1 regulators are put into low quiescent current mode, VCORE enters LDO mode, and the VANA and VFLASH2 regulators are disabled. All RF regulators are disabled during sleep mode. When the SLEEPX signal is detected high by the UEMC, the mobile terminal enters active mode and all functions are activated.

Sleep mode is exited either by the expiration of a sleep clock counter in the UEMC or by some external interrupt (generated by a charger connection, key press, headset connection, etc.). The VCTCXO is shut down in sleep mode and the 32 kHz sleep clock oscillator is used as a reference clock for the baseband.

Active Mode

In active mode, the mobile terminal operates normally by scanning for channels, listening to a base station, and transmitting and processing information. There are several sub-states in the active mode depending on the mobile terminal present state of the mobile terminal, such as burst reception, burst transmission etc.

In active mode, software controls the UEMC RF regulators: VR1A and VR1B can be enabled or disabled. VSIM can be enabled or disabled and its output voltage can be programmed to be 1.8 V or 3.3 V. VR2 and VR4—VR7 can be enabled or disabled or forced into low quiescent current mode. VR3 is always enabled in active mode and disabled during sleep mode and cannot be controlled by software in the same way as the other regulators. VR3 only turns off if both processors request to be in sleep mode.

Charging Mode

Charging mode can function in parallel with any other operating mode. A BSI resistor inside the battery pack indicates the battery type/size. The resistor value corresponds to a specific battery capacity. The UEMC measures the battery voltage, temperature, size, and charging current.

CHACON inside the UEMC controls the charging current delivered from the charger to the battery and mobile terminal. The battery voltage rise is limited by turning the UEMC switch off when the battery voltage has reached 4.2 V. The charging current is monitored by measuring the voltage drop across a 220 mOhm resistor.

Power Distribution

In normal operation, the baseband is powered from the mobile terminal's battery. The battery consists of one lithium-ion cell capacity of 1070 mAh and some safety and protection circuits.

The UEMC ASIC controls the power distribution to the whole mobile terminal through the baseband and RF regulators excluding the power amplifier (PA), which has a continuous power rail directly from the battery. The battery feeds power directly to the following parts of the system:

- UEMC
- PA
- Vibra
- Display
- Keyboard lights

The heart of the power distribution is the power control block inside the UEMC. It includes all the voltage regulators and feeds the power to the entire system. The UEMC handles hardware power-up functions so the regulators are not powered and the power up reset (PURX) is not released if the battery voltage is less than 3 V.

The baseband is powered from the following UEMC regulators:

Table 1: Baseband Regulators

Regulator	Maximum Current (mA)	Vout (V)	Notes
VCORE	300	1.35/1.05	Power up default 1.35V and 1.05V in sleep mode.
VIO	150	1.8	Enabled always except during power-off mode
VFLASH1	70	2.78	Enabled always except during power-off mode
VFLASH2	40	2.78	Enabled only when data cable is connected
VANA	80	2.78	Enabled only when the system is awake (Off during sleep and power-off modes)
VSIM	25	3.0	Enabled only when SIM card is used

Table 2 includes the UEMC regulators for the RF.

Table 2: RF Regulators

Regulator	Maximum Current (mA)	Vout (V)	Notes
VR1A	10	4.75	Enabled when cell transmitter is on
VR1B	10	4.75	Enabled when the transmitter is on
VR2	100	2.78	Enabled when the transmitter is on
VR3	20	2.78	Enabled when SleepX is high
VR4	50	2.78	Enabled when the receiver is on
VR5	50	2.78	Enabled when the receiver is on
VR6	50	2.78	Enabled when the transmitter is on
VR7	45	2.78	Enabled when the receiver is on

The charge pump that is used by VR1A is constructed around the UEMC. The charge pump works with the CBUS oscillator (1.2 MHz) and gives a 4.75 V regulated output voltage to the RF.

Clock Distribution

RFClk (19.2 MHz Analog)

The main clock signal for the baseband is generated from the voltage and temperature controlled crystal oscillator (VCTCXO) and sent to the UPP at pin M5.

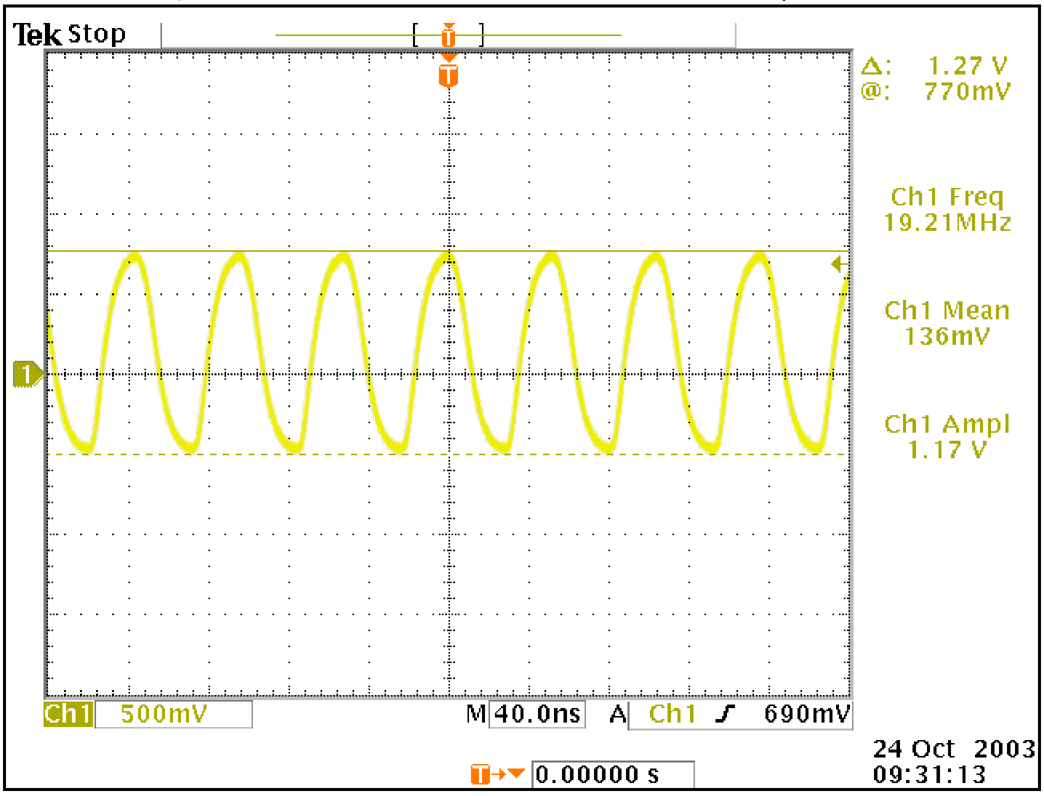


Figure 4: Waveform of the 19.2 MHz clock (VCTCXO) going to the UPP

RFConvClk (19.2 MHz digital)

The UPP distributes the 19.2 MHz internal clock to the DSP and MCU, where the software multiplies this clock by seven for the DSP and by two for the MCU.

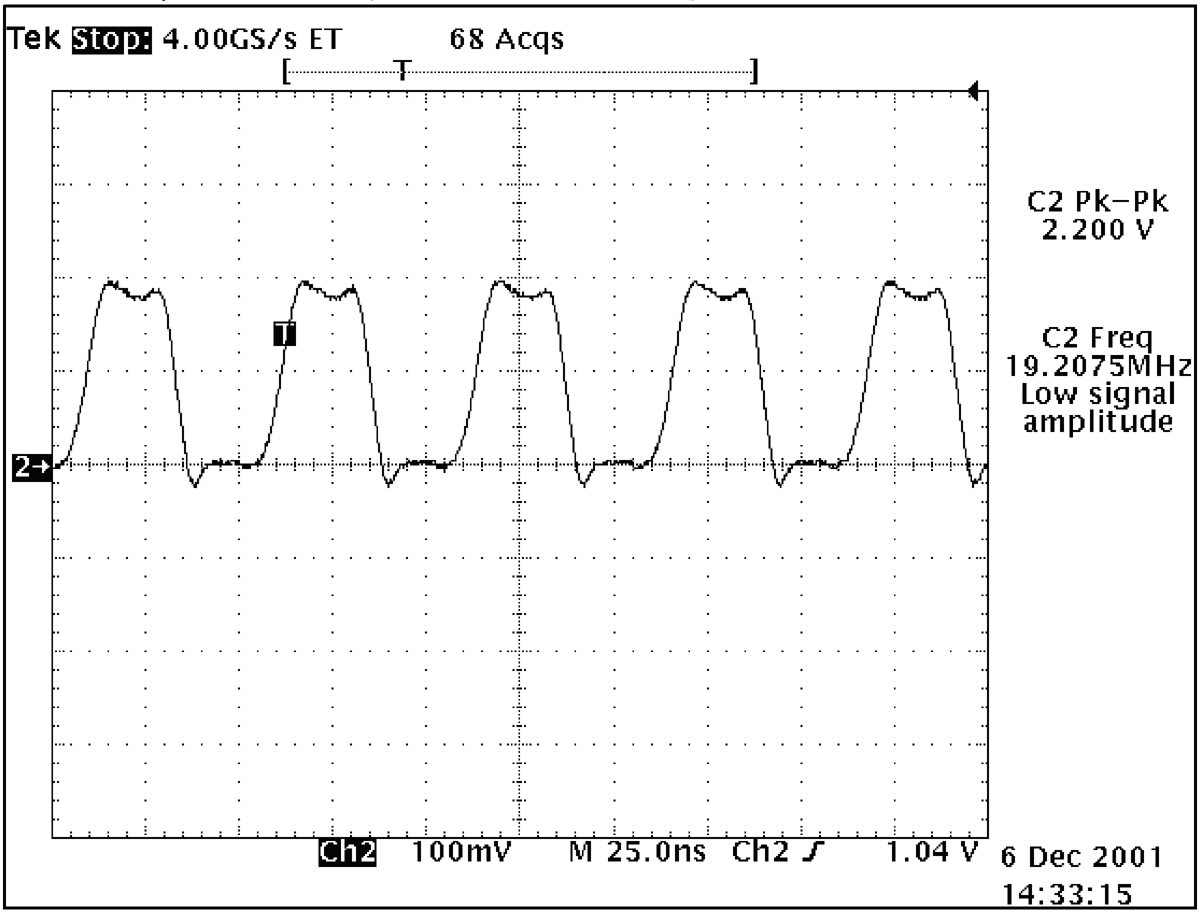


Figure 5: RFCovCLk waveform

CBUS Clk Interface

A 1.2 MHz clock signal is used for CBUS, which is used by the MCU to transfer data between the UEMC and the UPP.

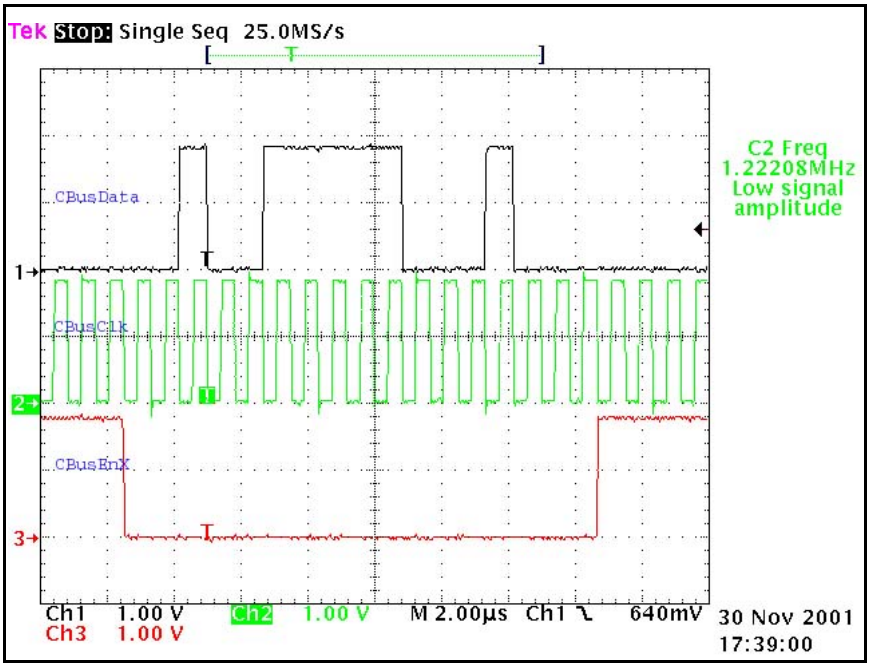


Figure 6: CBUS data transfer

DBUS Clk Interface

A 9.6 MHz clock signal is used for DBUS, which is used by the DSP to transfer data between the UEMC and UPP.

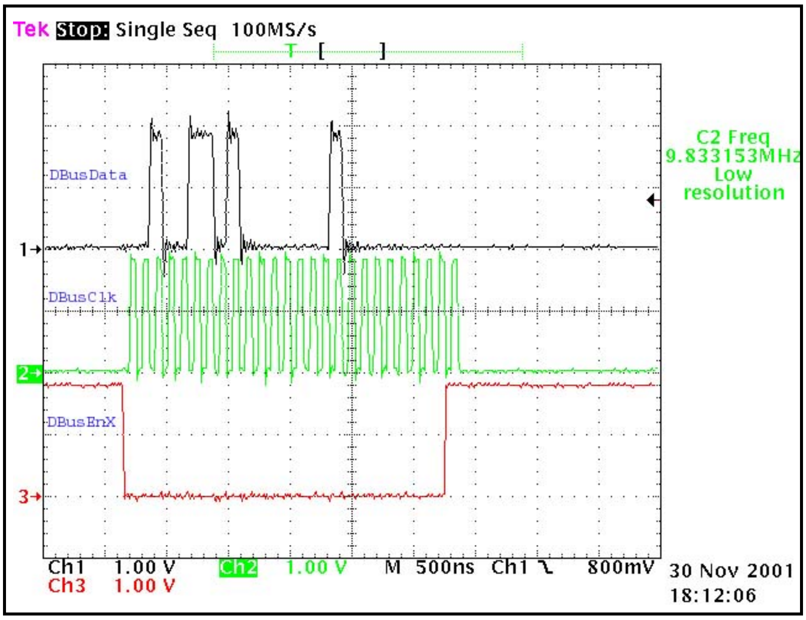


Figure 7: DBUS data transferring

The system clock is stopped during sleep mode by disabling the VCTCXO power supply (VR3) from the UEMC regulator output by turning off the controlled output signal SleepX from the UPP.

SleepCLK (Digital)

The 32 kHz sleep clock in the UEMC is also used in the UPP for sleep mode timing.

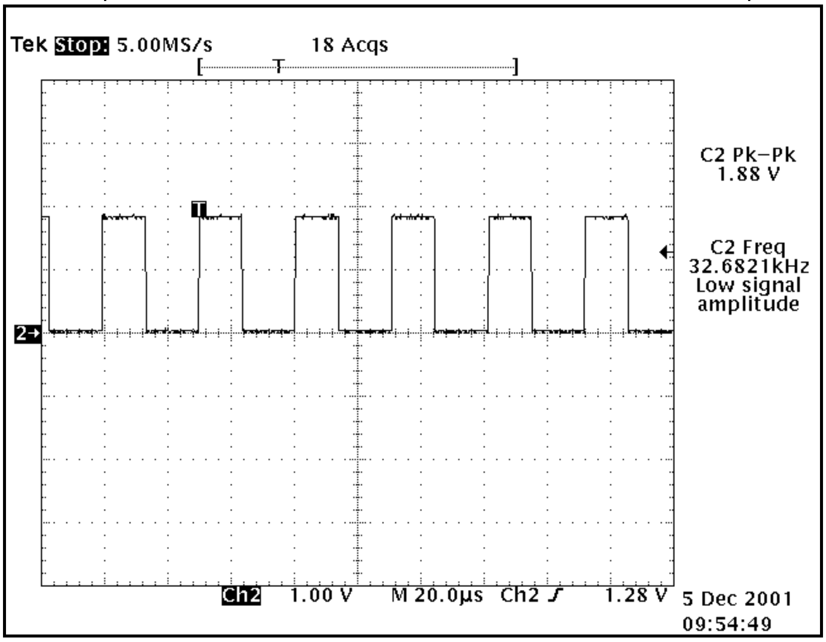


Figure 8: 32 kHz Digital output from UEMC

SleepCLK (Analog)

When the system enters sleep mode or power off mode, the external 32 KHz crystal provides a reference to the UEMC RTC circuit to turn on the mobile terminal during power-off or sleep mode.

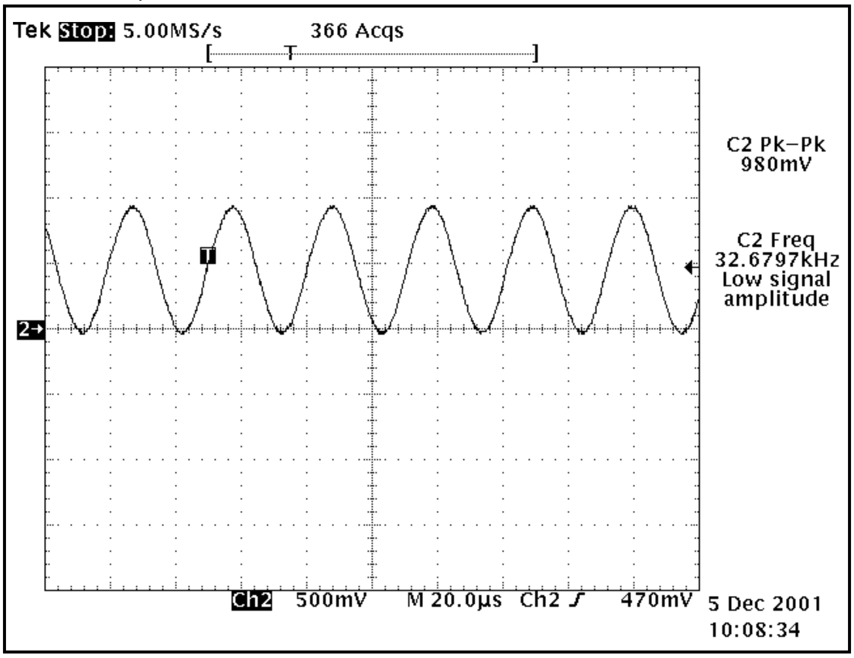


Figure 9: 32 kHz analog waveform at the 32 KHz crystal input

Flash Programming Error Codes

The following characteristics apply to the information in Table 3.

- Error codes can be seen from the test results or from Phoenix's flash-tool.
- Underlined information means that the connection under consideration is being used for the first time.

Table 3: Flash Programming Error Codes

Error	Description	Not Working Properly
C101	"The Phone does not set FbusTx line high after the startup."	Vflash1 VBatt BSI and FbusRX from prommer to UEMC. FbusTx from UPP->UEMC->Prommer(SA0)
C102	"The Phone does not set FbusTx line low after the line has been high. The Prommer generates this error also when the Phone is not connected to the Prommer."	PURX(also to Safari) VR3 Rfclock(VCTCXO->Safari->UPP) Mbus from Prommer->UEMC->UPP(MbusRx)(SA0) FbusTx from UPP->UEMC->Prommer(SA1) BSI and FbusRX from prommer to UEMC.
C103	" Boot serial line fail."	Mbus from Prommer->UEMC->UPP(MbusRx)(SA1) FbusRx from Prommer->UEMC->UPP FbusTx from UPP->UEMC->Prommer
C104	"MCU ID message sending failed in the Phone."	FbusTx from UPP->UEMC->Prommer
C105	"The Phone has not received Secondary boot codes length bytes correctly."	Mbus from Prommer->UEMC->UPP(MbusRx) FbusRx from Prommer->UEMC->UPP FbusTx from UPP->UEMC->Prommer
C106	"The Phone has not received Secondary code bytes correctly."	Mbus from Prommer->UEMC->UPP(MbusRx) FbusRx from Prommer->UEMC->UPP FbusTx from UPP->UEMC->Prommer
C107	"The Phone MCU can not start Secondary code correctly."	UPP
C586	"The erasing status response from the Phone informs about fail."	Flash
C686	"The programming status response from the Phone informs about fail."	Flash
Cx81	"The Prommer has detected a checksum error in the message, which it has received from the Phone."	FbusTx from UPP->UEMC->Prommer
Cx82	"The Prommer has detected a wrong ID byte in the message, which it has received from the Phone."	FbusTx from UPP->UEMC->Prommer

Table 3: Flash Programming Error Codes (Continued)

Error	Description	Not Working Properly
A204 Cx83 Cx84 Cx85	"The flash manufacturer and device IDs in the existing algorithm files do not match with the IDs received from the target phone." "The Prommer has not received phone acknowledge to the message." "The phone has generated NAK signal during data block transfer." "Data block handling timeout"	Flash UPP VIO/VANA Signals between UPP-Flash Mbus from Prommer->UEMC->UPP(MbusRx) FbusRx from Prommer->UEMC->UPP FbusTx from UPP->UEMC->Prommer
Cx87	"Wrong MCU ID."	RFClock UPP(Vcore)
Startup for flashing	Required startup for flashing	Vflash1 VBatt

Charging Operation

Battery

The 2115i/2116/2116i uses a Lithium-Ion cell battery with a capacity of 1070 mAh. Reading a resistor inside the battery pack on the BSI line indicates the battery size. The mobile terminal measures the approximate temperature of the battery on the BTEMP line with an NTC resistor on the PCB.

The temperature and capacity information are needed for charge control. These resistors are connected to the BSI pin of the battery connector and the BTEMP of the mobile terminal. The mobile terminal has 100 kΩ pull-up resistors for this line so that they can be read by A/D inputs in the mobile terminal.

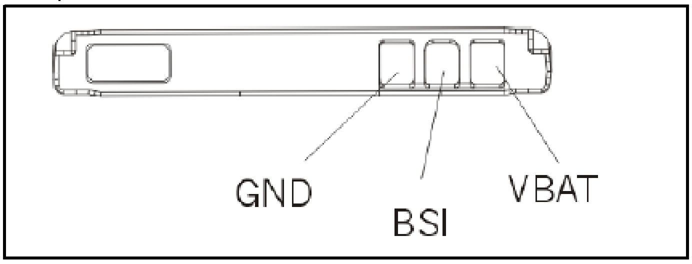


Figure 10: BL-6C battery pack pin order

Charging Circuitry

The UEMC ASIC charge control is dependent on the charger type and the battery size. External components are needed for electromagnetic compatibility (EMC), reverse polarity, and transient protection of the input to the baseband module. The charger connection is through the system connector interface. The baseband supports DCT3 chargers, including both 2- and 3-wire type chargers. However, 3-wire chargers are treated as 2-wire chargers.

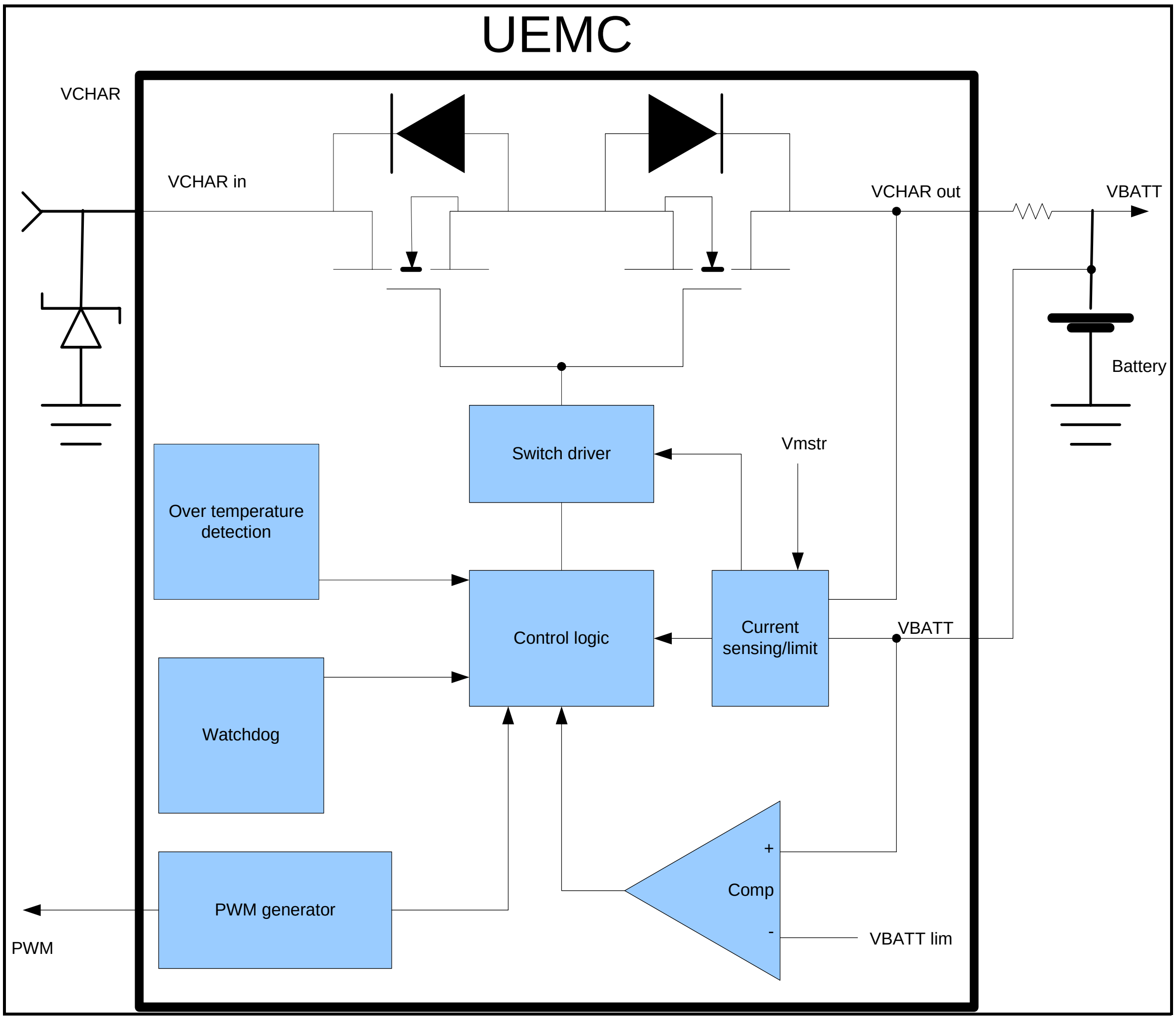


Figure 11: Charging circuitry

Charger Detection

Connecting a charger creates voltage on the VCHAR input of the UEMC. Charging starts when the UEMC detects the VCHAR input voltage level above 2 V (VCHdet+ threshold). The VCHARDET signal is generated to indicate the presence of the charger for the software. The energy management (EM) software controls the charger identification/acceptance. The charger recognition is initiated when the EM software receives a "charger connected" interrupt. The algorithm basically consists of the following three steps:

1. Check that the charger output (voltage and current) is within safety limits.
2. Identify the charger as a 2- or 3-wire charger.
3. Check that the charger is within the charger window (voltage and current).

If the charger is accepted and identified, the appropriate charging algorithm is initiated.

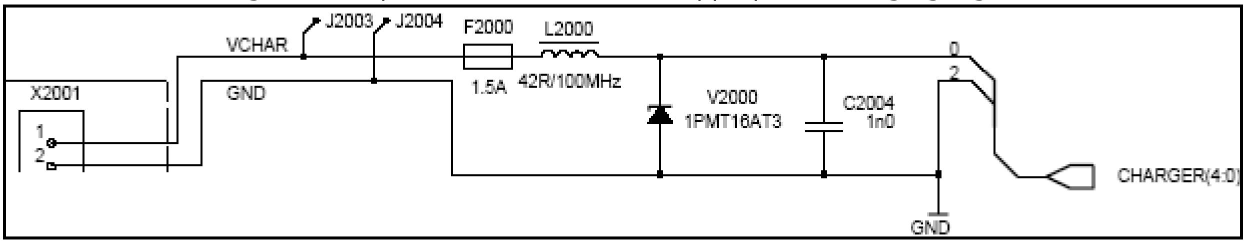


Figure 12: Charging circuit

Charge Control

In active mode, charging is controlled by the UEMC's digital part. Charging voltage and current monitoring are used to limit charging into a safe area. The UEMC has the following programmable charge cut-off limits:

- VBATLim1 = 3.6 V (Default)
- VBATLim2L = 5.0 V
- VBATLim2H = 5.25 V

VBATLim1, 2L, and 2H are designed with hystereses. When the voltage rises above VBATLim1, 2L, 2H+, charging is stopped by turning off the charging switch. No change is done in operational mode. Charging restarts after the voltage has decreased below VBATLim-.

There are two pulse-width modulation (PWM) frequencies in use depending on the type of the charger. A 2-wire charger uses a 1 Hz, while a 3-wire charger uses a 32 Hz. The duty cycle range is 0% to 100%. The maximum charging current is limited to 1.2 A.

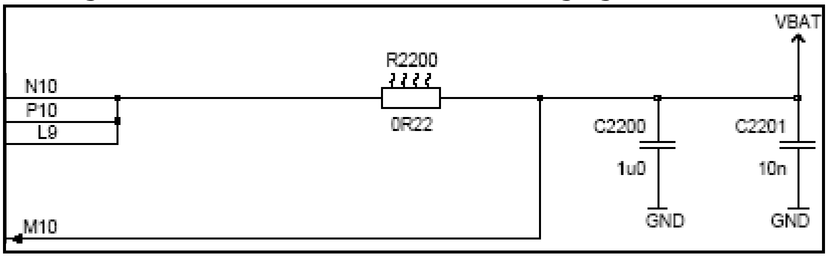


Figure 13: Charging circuity at the battery

Audio

The audio control and processing is provided by the UEMC, which contains the audio codec, and the UPP, which contains the MCU and DSP blocks. These blocks handle and process the audio data signals. The baseband supports three microphone inputs and two earpiece outputs.

MIC1 input is used for the mobile terminal's internal microphone. MIC2 input is used for headsets. MIC3 is not used. Every microphone input can have either a differential or single-ended AC connection to the UEMC circuit. The internal microphone (MIC1) and external microphone (MIC2) for Pop-port™ accessory detection are both differential. The microphone signals from different sources are connected to separate inputs at the

UEMC. Inputs for the microphone signals are differential types. Also, MICBIAS1 is used for MIC1 and MICBIAS2 is used for MIC2. The 2115i/2116/2116i also support a hands-free speaker, which is driven by an IHF audio amplifier.

Display and Keyboard

The mobile terminal uses light-emitting diodes (LEDs) for liquid crystal display (LCD) and keypad illumination. There is one LED for the LCD and four LEDs for the keypad. KLIGHT is the signal used to drive the LED driver for the LCD and keyboard. This signal turns on the LED driver (N2400).

The mobile terminal also uses an IOS LCD. The interface uses a 9-bit data transfer and is quite similar to the DCT3 type interface, except the Command/Data information is transferred together with the data.

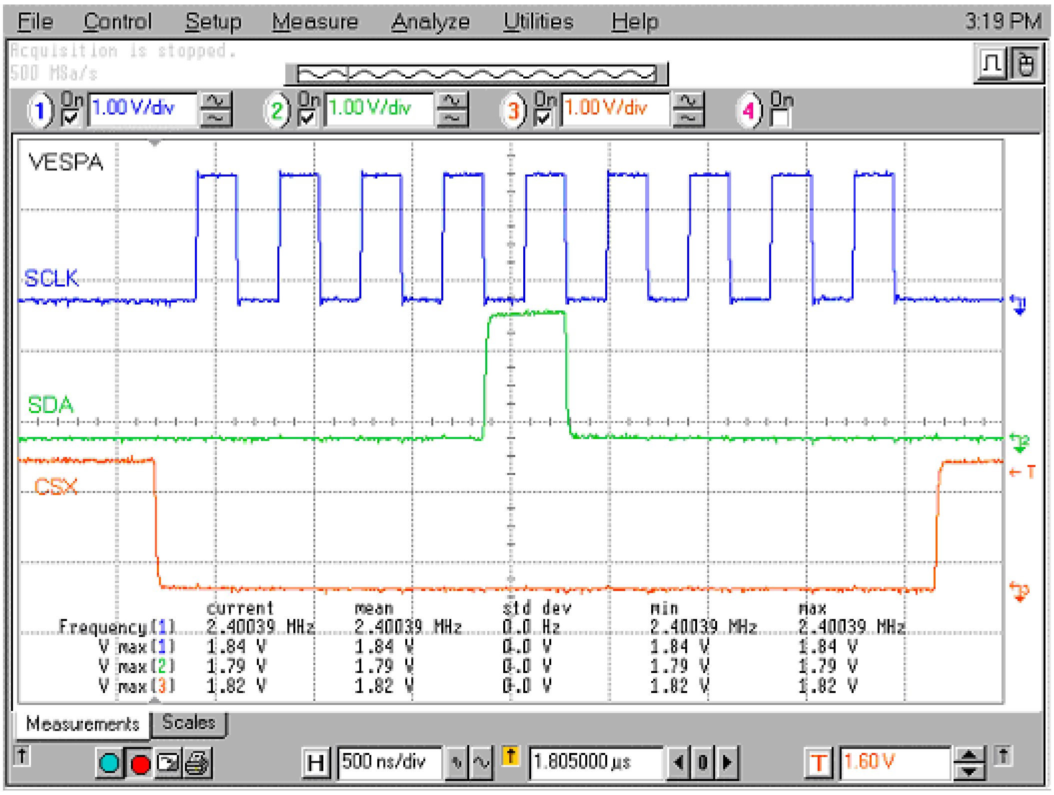


Figure 14: Waveform for the LCD Interface

Flashlight

The flashlight is driven by the white LED driver and controlled by the UEMC. The TK65600B-G is an active-high enable device, which is tied to the DLIGHT signal from the UEMC.

Accessories

The 2115i/2116/2116i supports Pop-port accessories. Detection of the accessories is done through the ACI signal.

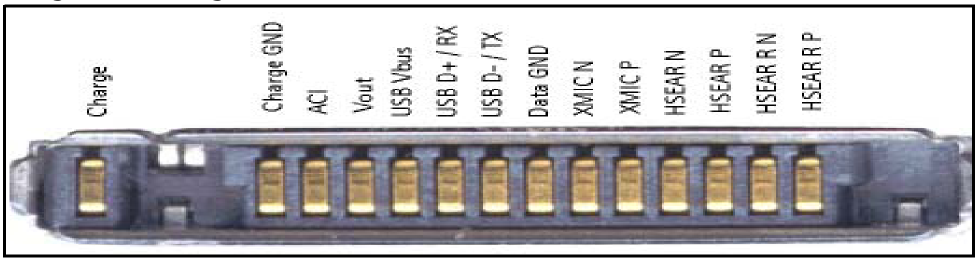


Figure 15: Pop-port connector pin out

The pin out on the Pop-port connector is as follows:

- Charger
- Charger GND
- ACI
- Vout
- USB Vbus
- USB D+ / Fbus Rx
- USB D- / Fbus Tx
- Data GND
- XMic N
- XMic P
- HSear N
- HSear P
- HSear R N
- HSear R P

You can perform the following in Pop-port accessories:

- Charging
- Accessory detection
- FBUS communication
- Fully differential audio interface for mono and stereo outputs

Charging

Charging through the Pop-port connector is accomplished in the same manner as through the charger connector. Pin 1 is physically connected to the charger connector. When the mobile terminal is connected to a desktop charger, it charges in the same manner as it does with the charger connector.

Figure 16 shows the actual charging sequence. The channels shown are:

- CH1 = Charging current across the .22 Ohm (R2200) resistor on UEMK
- CH2 = Charger voltage measure at V2000
- CH3 = Battery voltage measure at R2200
- CH4 = PURX

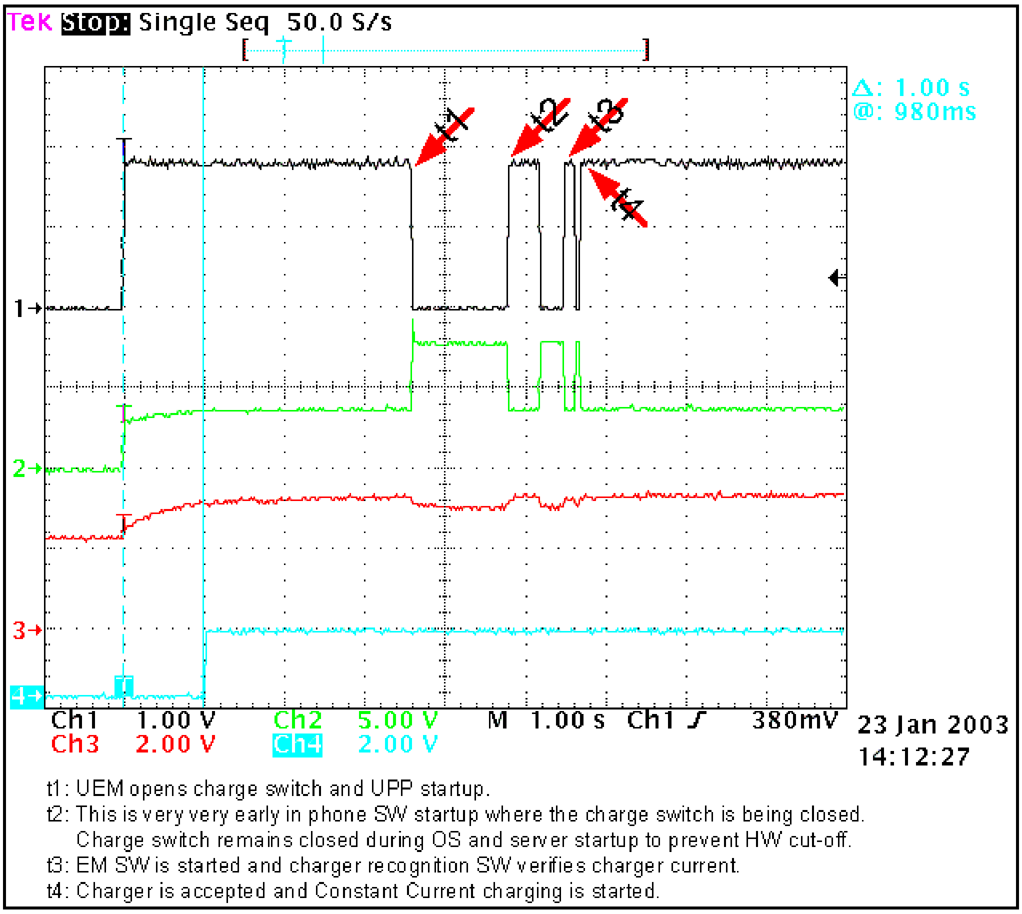


Figure 16: Charging sequence

In Channel 4, PURX is released, which shows when the mobile terminal operation goes from reset mode to power-on mode.

Pop-port Headset Detection

Accessory detection on the Pop-port is done digitally. The pins used for this accessory detection are:

- Pin 2 (Charge GND)
- Pin 3 (ACI)
- Pin 4 (Vout)

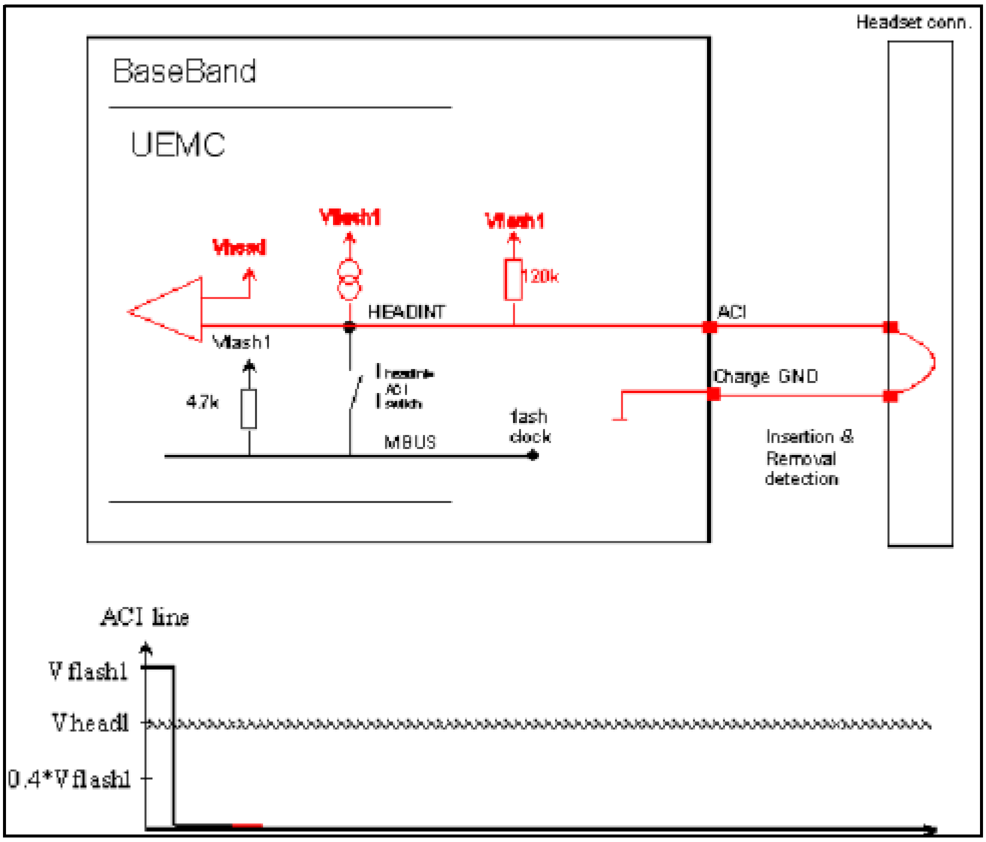


Figure 17: Waveform showing Pop-port accessory detection

FBUS Detection

FBUS communication in Pop-port is done through the following lines:

- Pin 2 (Charge GND)
- Pin 3 (ACI)
- Pin 4 (Vout)
- Pin 6 (FBUS Rx)
- Pin 7 (FBUS Tx)

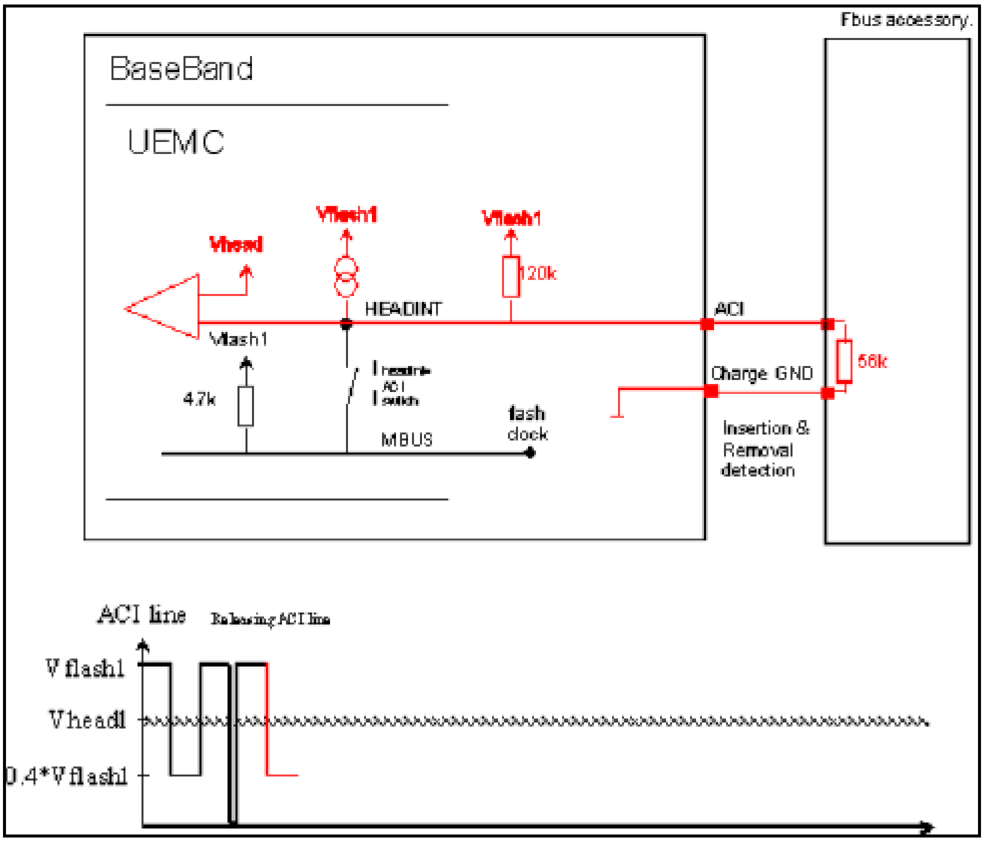


Figure 18: Waveform showing Pop-port FBUS communication

Accessory Detection Through ACI

USB and audio on (mono or stereo)/FM radio communication in Pop-port is done through the following signals:

Table 4: Accessory Detection Signals

USB	Audio/FM
Pin 5 (USB Vbus)	Pin 9 (XMic N)
Pin 6 (USB +)	Pin 10 (SMIC P)
Pin 7 (USB -)	Pin 11 (HSEAR N)
Pin 8 (Data GND)	Pin 12 (HSEAR P)

Table 4: Accessory Detection Signals (Continued)

USB	Audio/FM
	Pin 13 (HSEAR R N)
	Pin 14 (HSEAR R P)

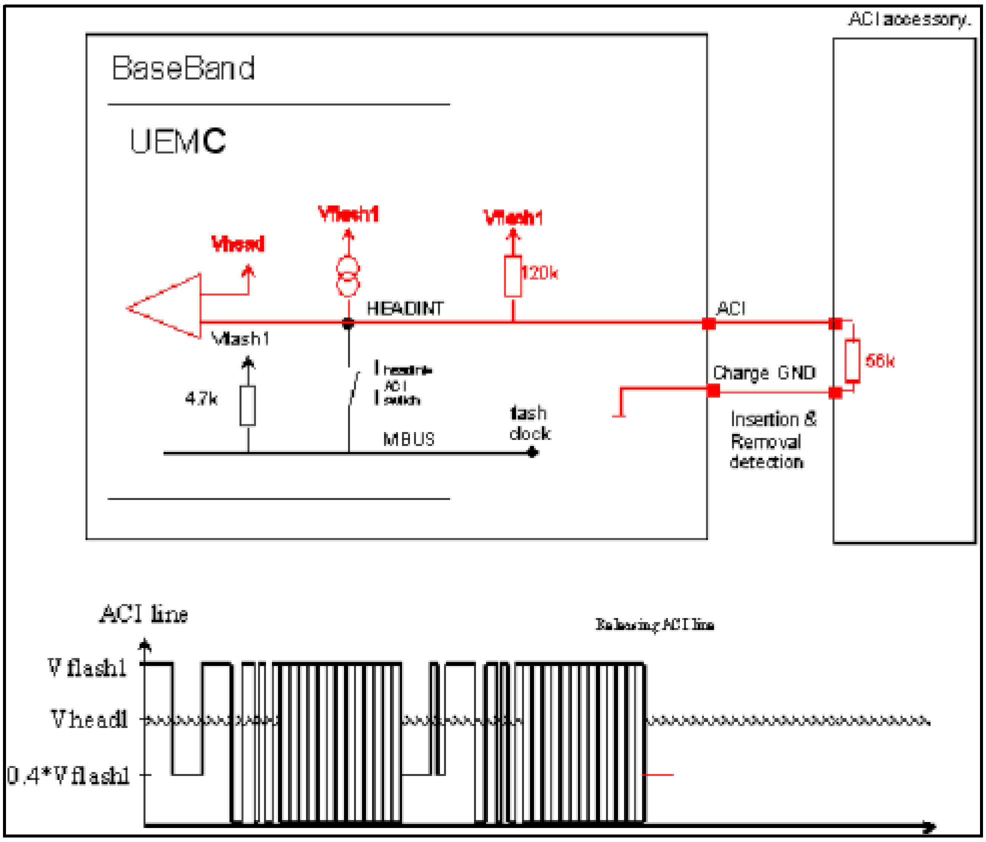


Figure 19: Waveform showing accessory detection through ACI

SIM CAR

The 2115i/2116/2116i supports SIM CAR. Use the waveform in Figure 20 to verify that the sim_vcc, sim_i/o, cim_clk, and sim_rst signals are activated in the correct sequence at power up. The figure shows the proper waveforms when the interface is working. See Figure 23 on page 32 for the test point's location.

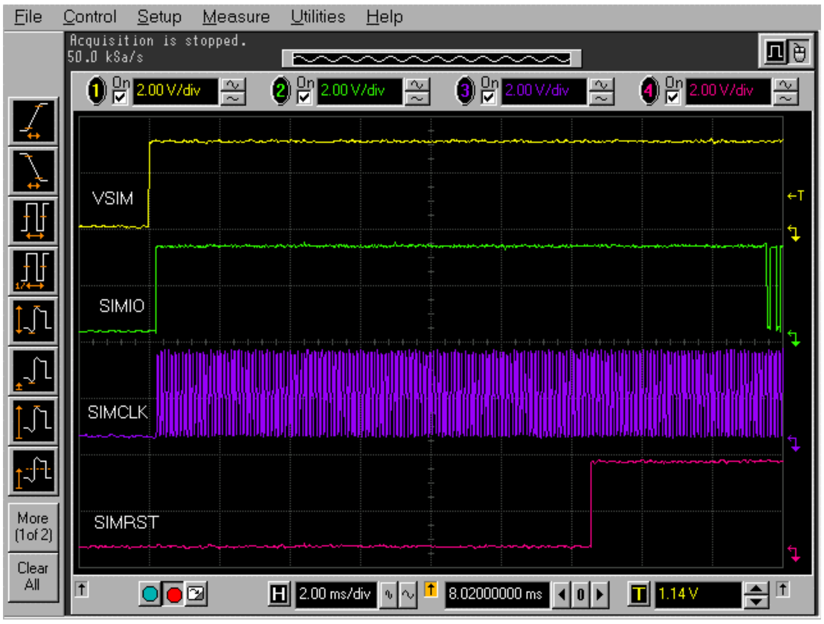


Figure 20: RUIM signal waveform

GPS Module

The GPS circuitry utilizes RF signals from satellites stationed in geosynchronous orbit to determine longitude and latitude of the mobile terminal. The GPS circuitry is completely separate of the CE circuitry and is located almost exclusively on the secondary side of the PWB underneath the display module. (See Figure 21 on page 30.)

Use the following steps for basic GPS BB troubleshooting:

1. Always perform a visual inspection on the GPS circuitry to see if the problem is physical (dislodged parts, corrosion, poor solder joints, etc.) before performing a diagnostic test.
2. Put the GE and CE in the proper mode.
3. Check to make sure that necessary inputs from the CE are good (power, clock, etc.).
4. Ensure that these inputs produce the proper outputs.

Because of the large level of integration (most functionality is contained in the two ASIC chips), the diagnostics you can perform are limited.

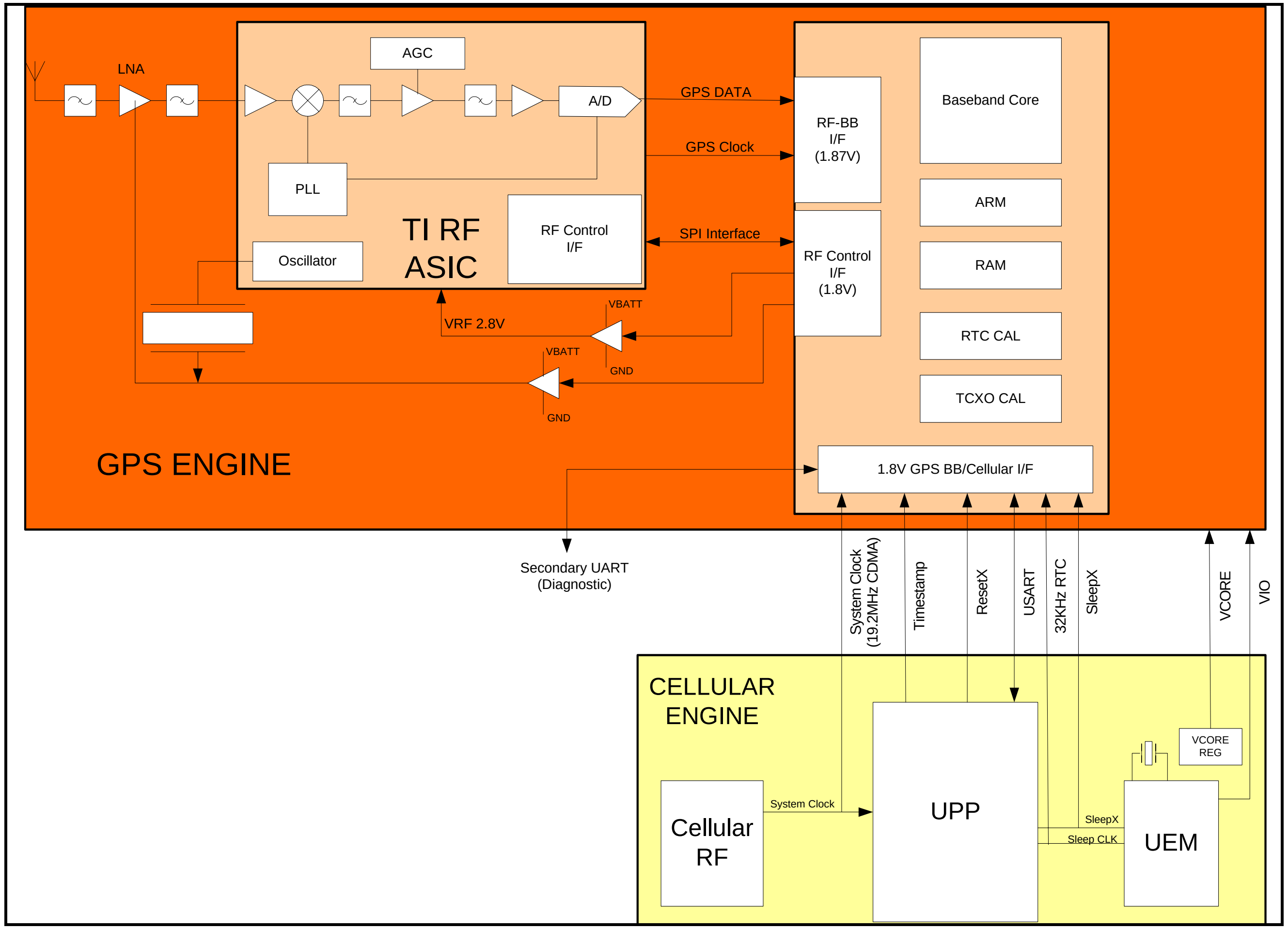


Figure 21: GPS block diagram

Test Points - Bottom

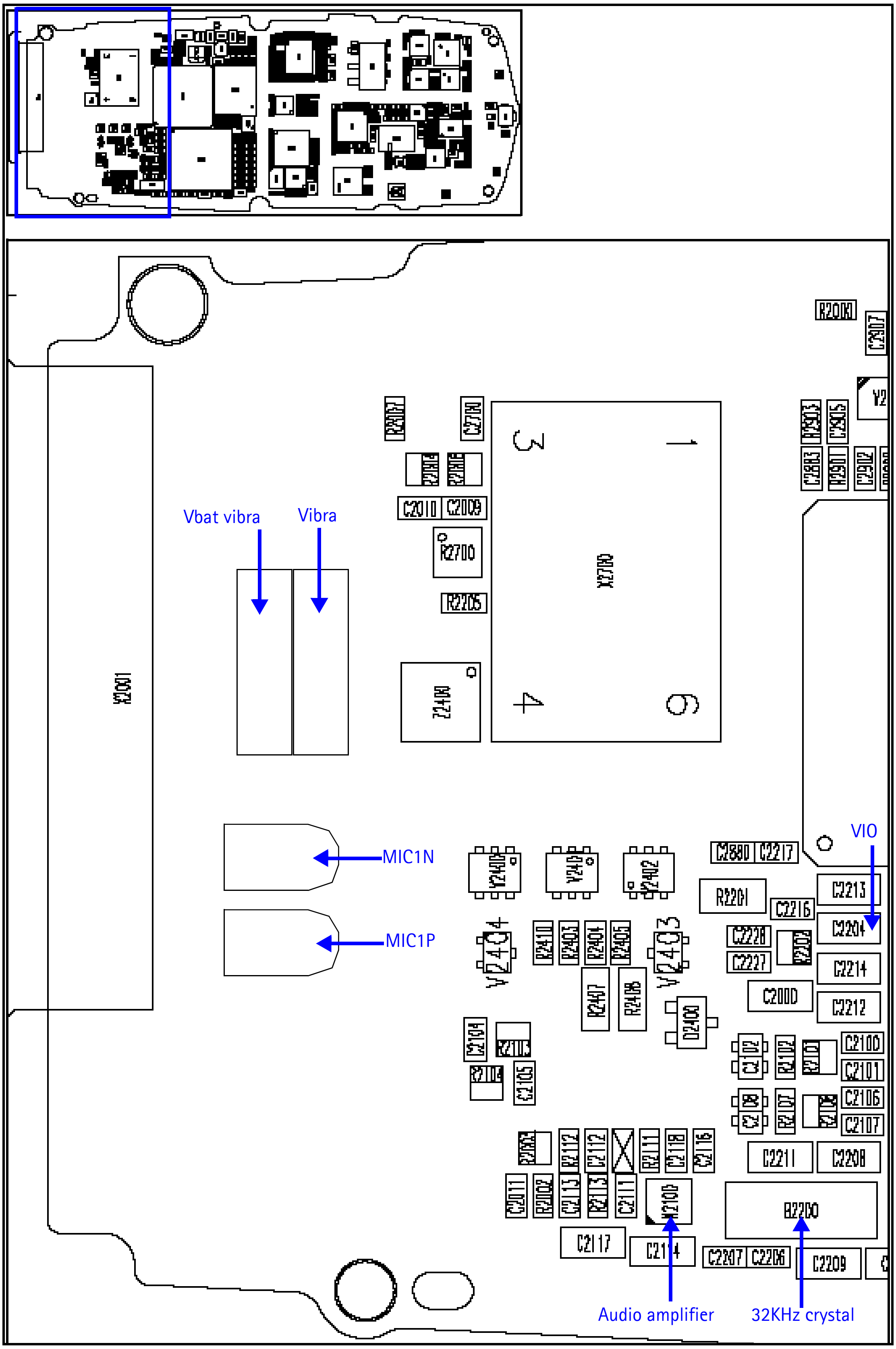


Figure 22: Test points (bottom 1)

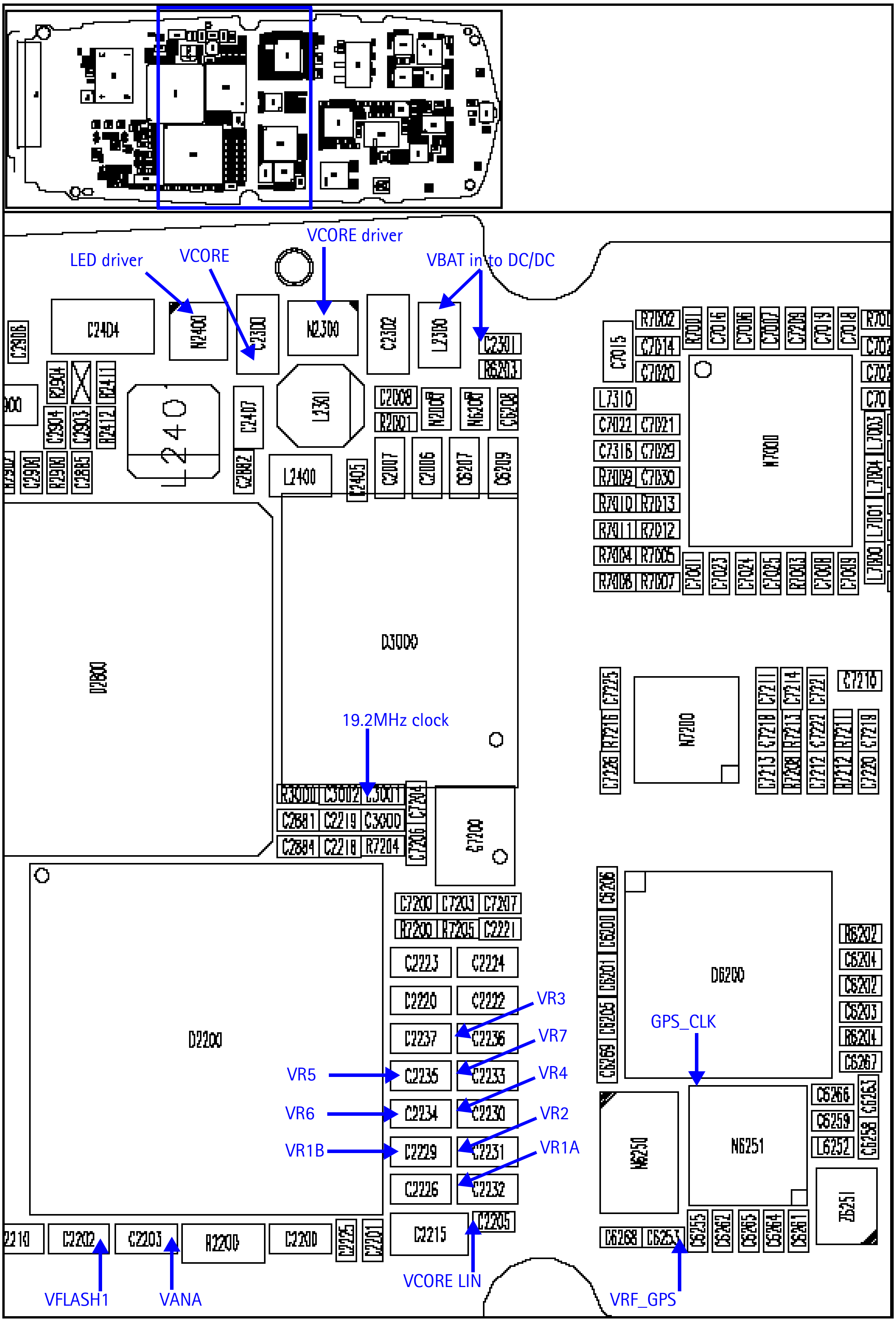


Figure 23: BB test points (bottom 2)

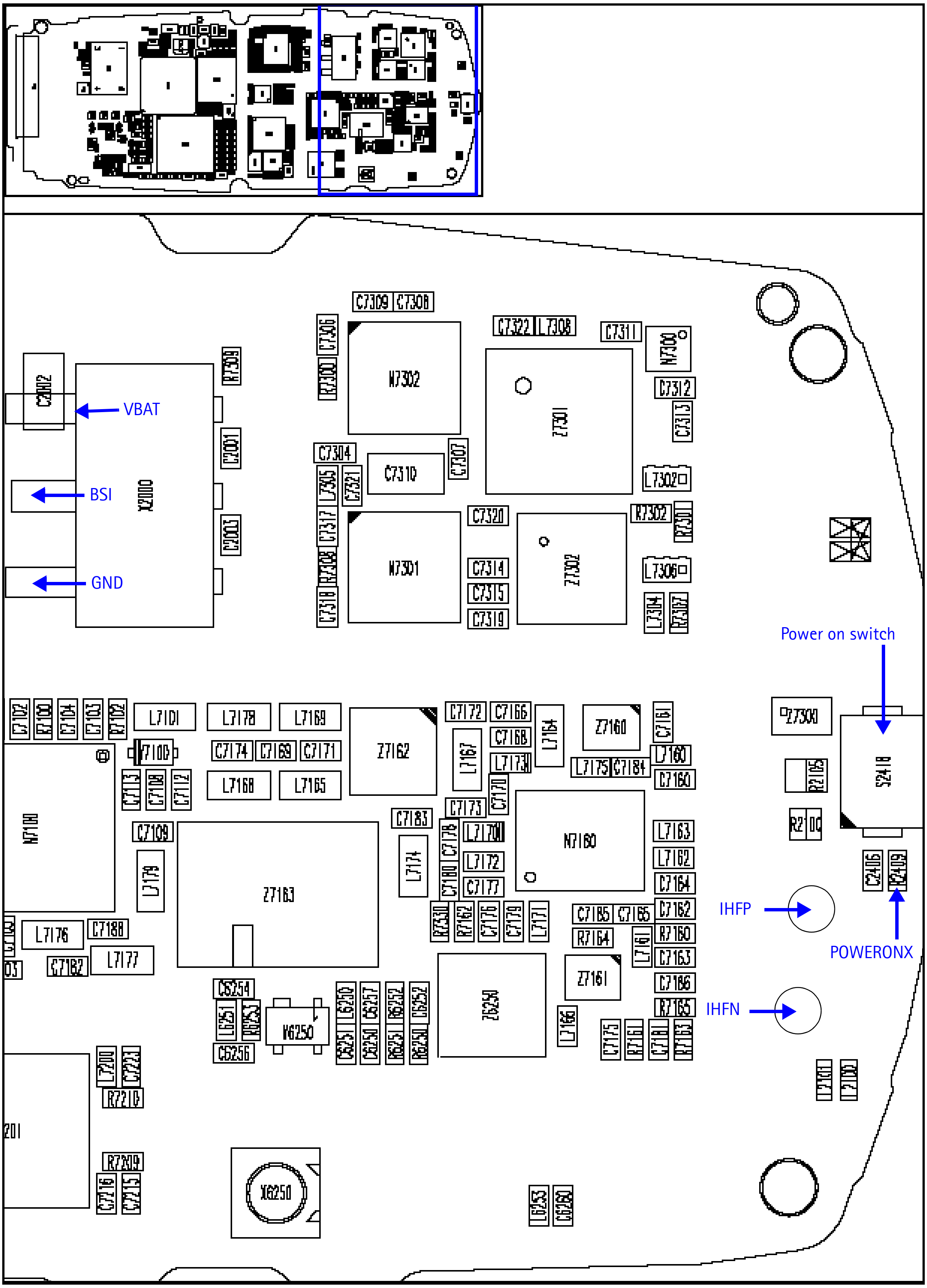


Figure 24: BB test points (bottom 3)

Test Points - Top

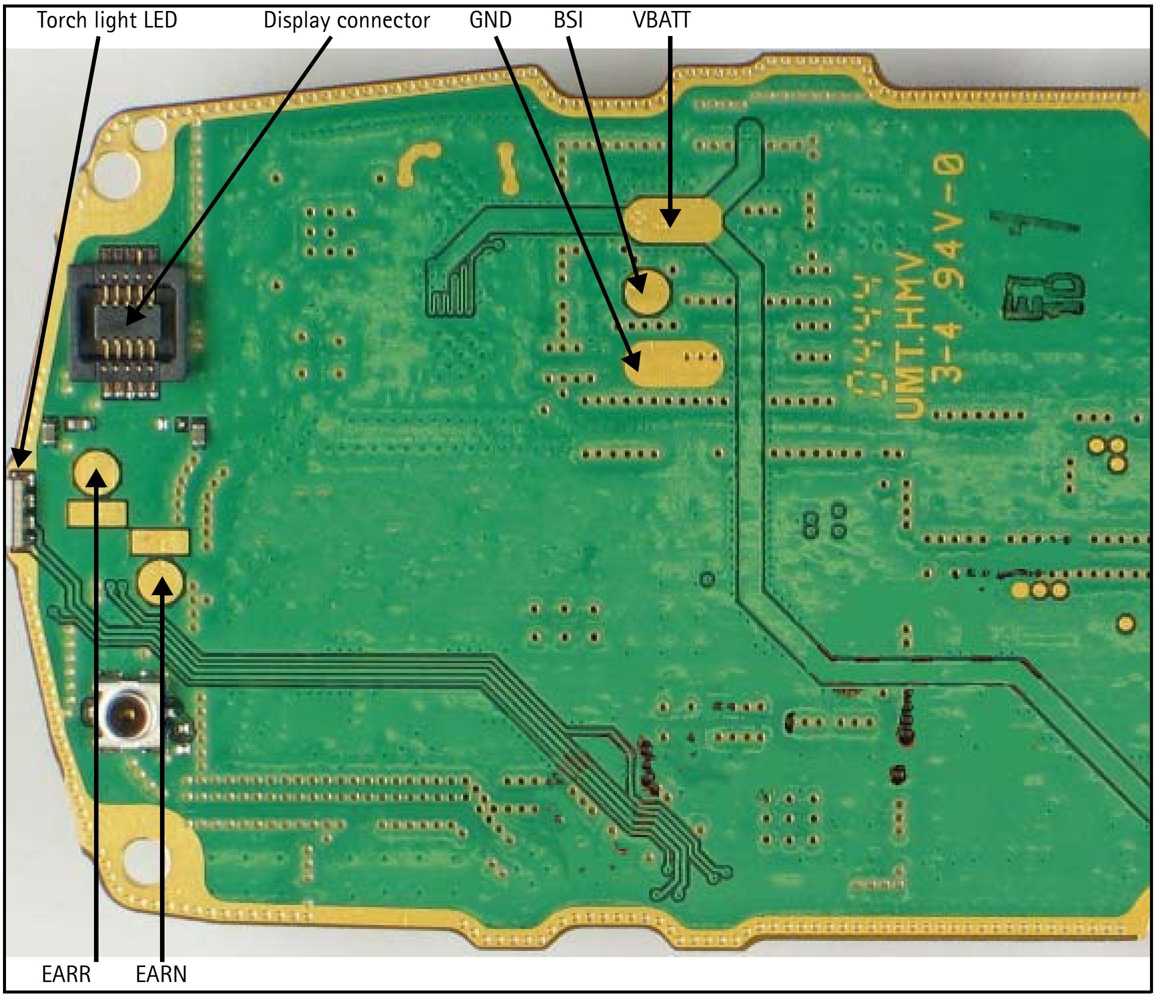


Figure 25: BB test points (top 1)

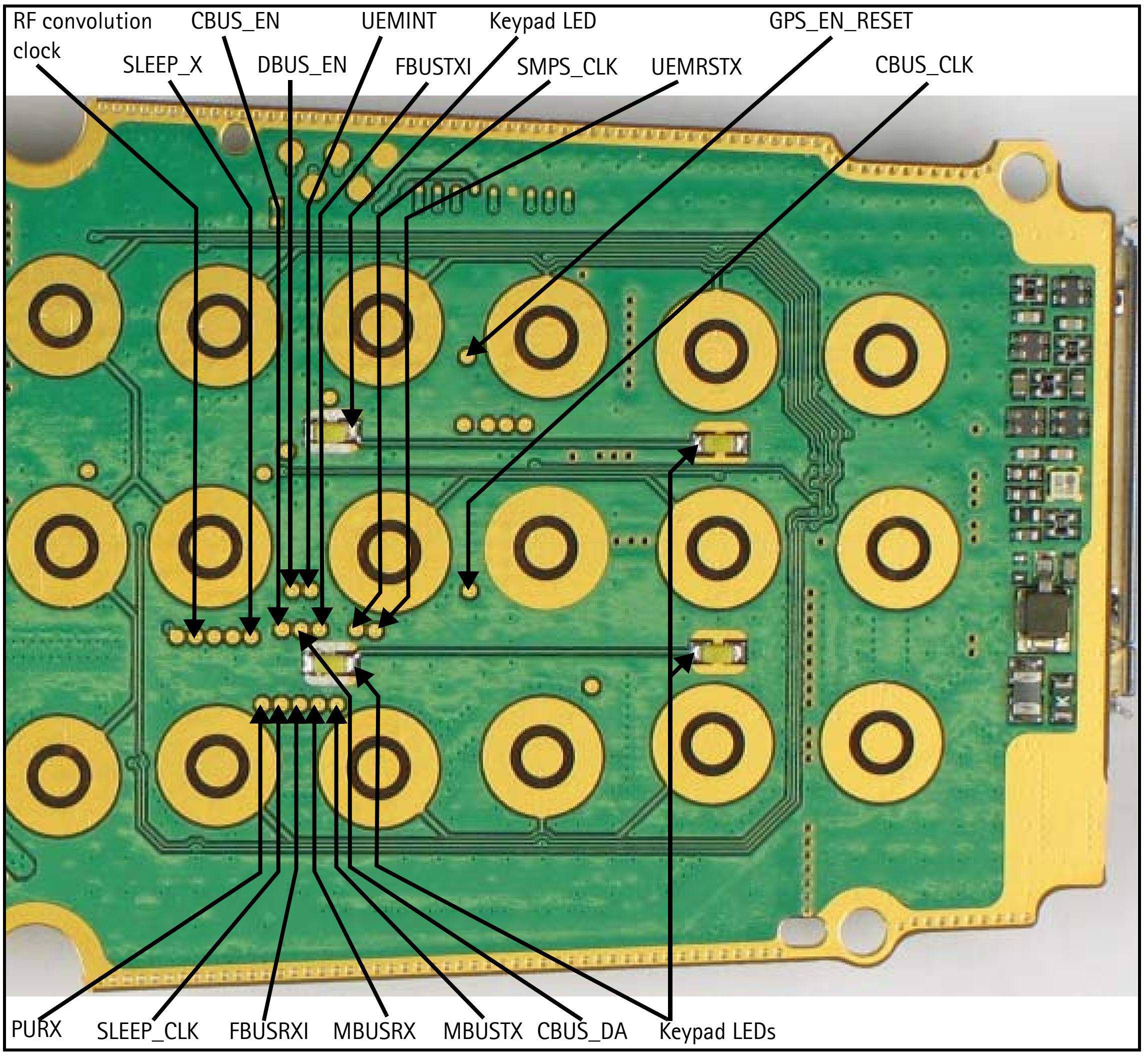


Figure 26: BB test points (top 2)

Troubleshooting

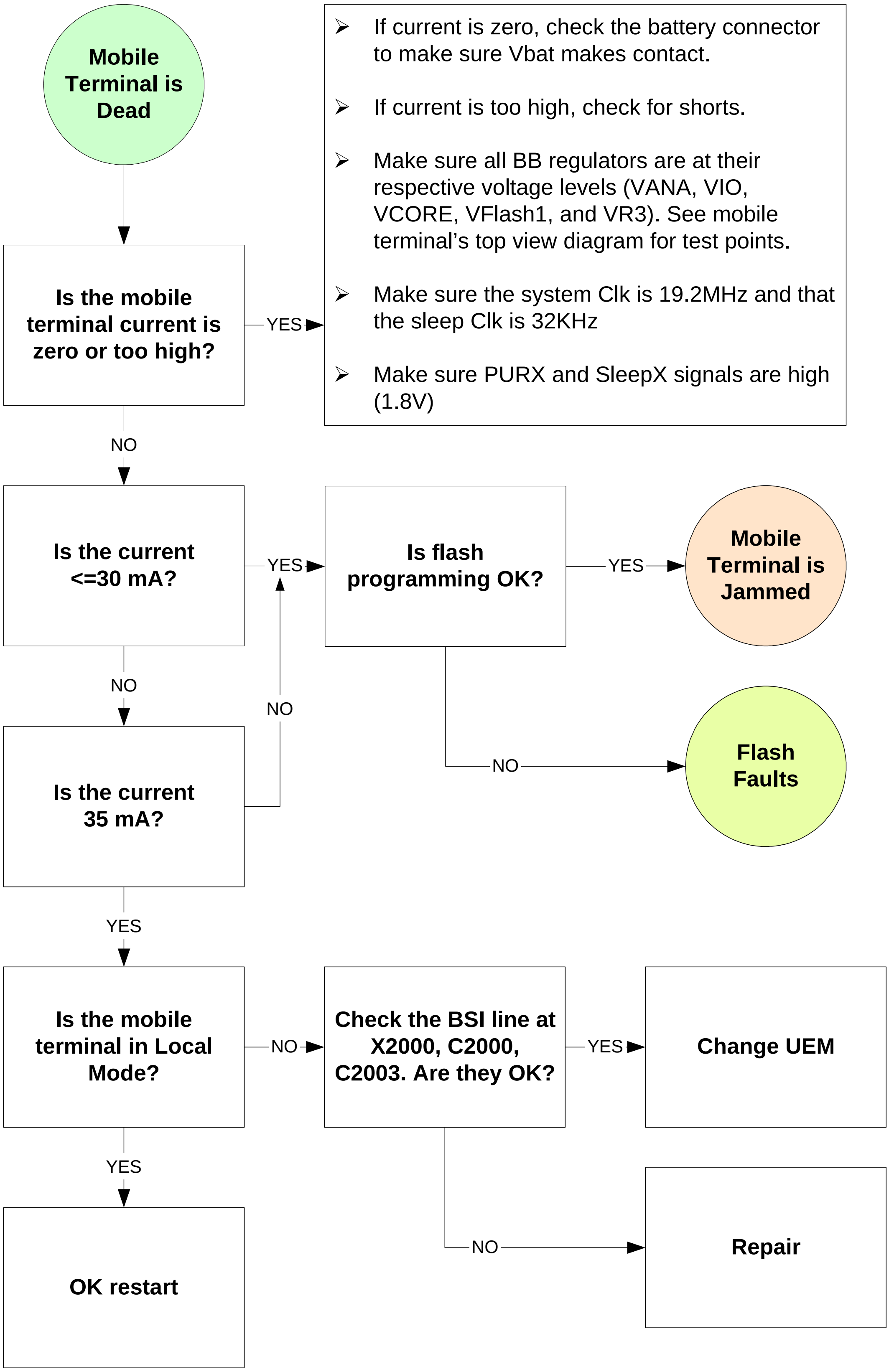
First, carry out a through visual check of the module. Ensure in particular that:

- There are no mechanical damages
- Soldered joints are okay
- ASIC orientations are okay

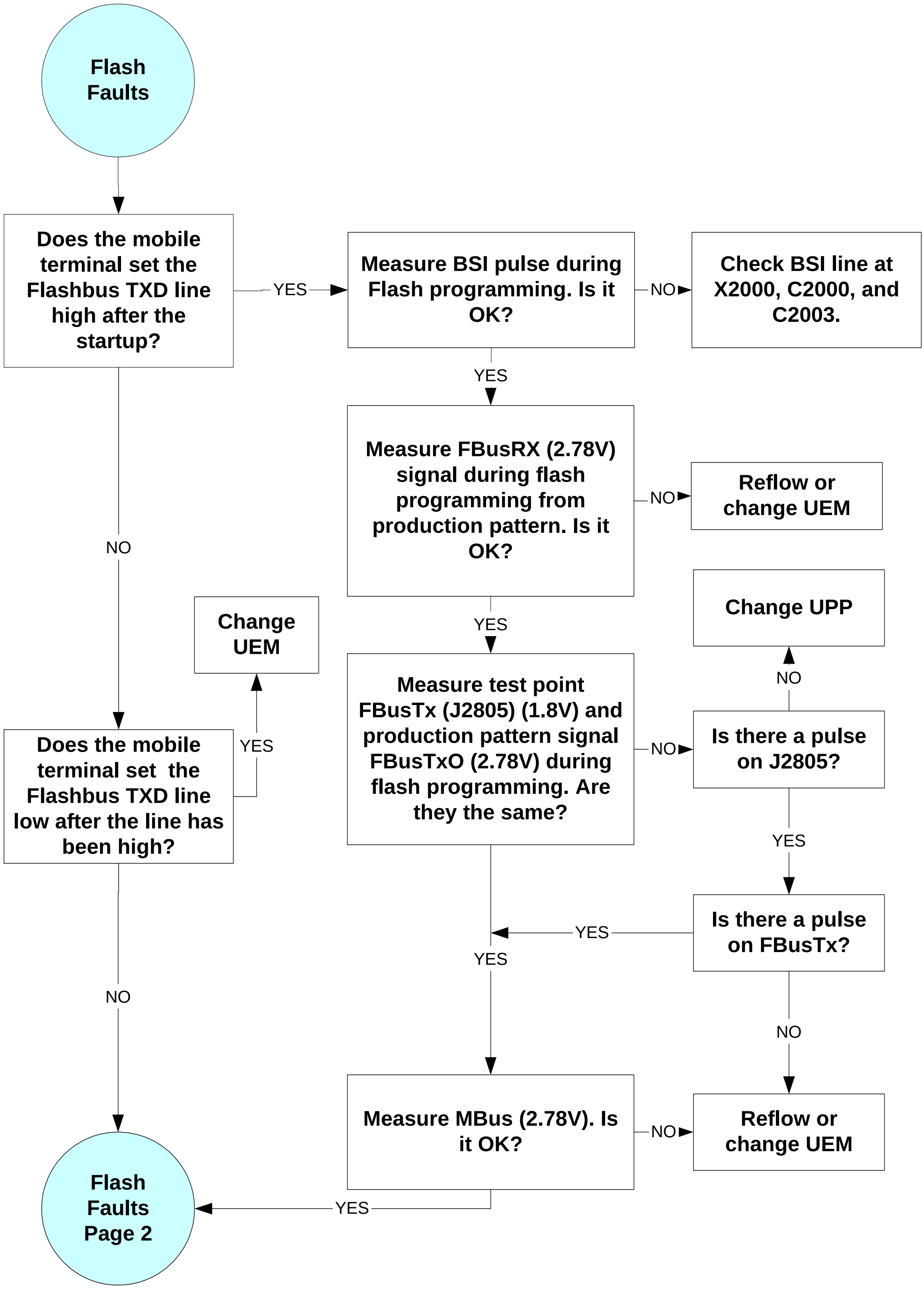
The following hints should help finding the cause of the problem when the circuitry seems to be faulty. Troubleshooting instructions are divided into the following sections:

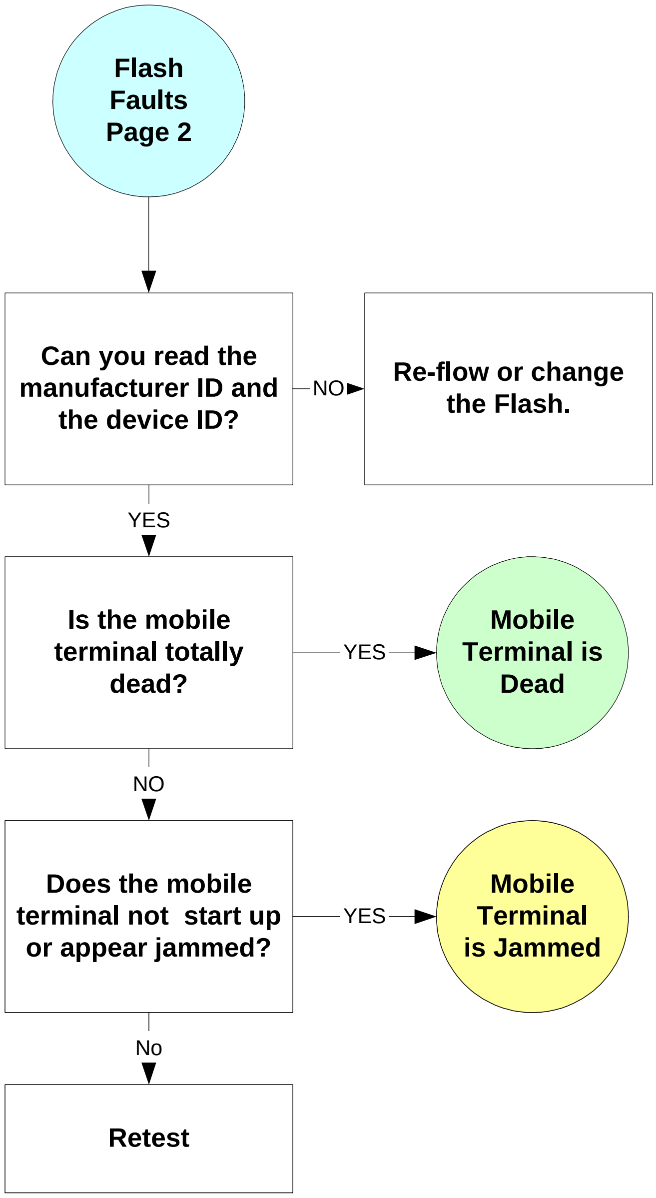
- "Mobile Terminal is Dead"
- "Flash Faults"
- "Power Does Not Stay on or the Mobile Terminal is Jammed"
- "Charger Faults"
- "Audio Faults"
- "Display Faults"
- "Keypad Faults"
- "Flashlight Faults"
- "GPS Faults"

Mobile Terminal is Dead

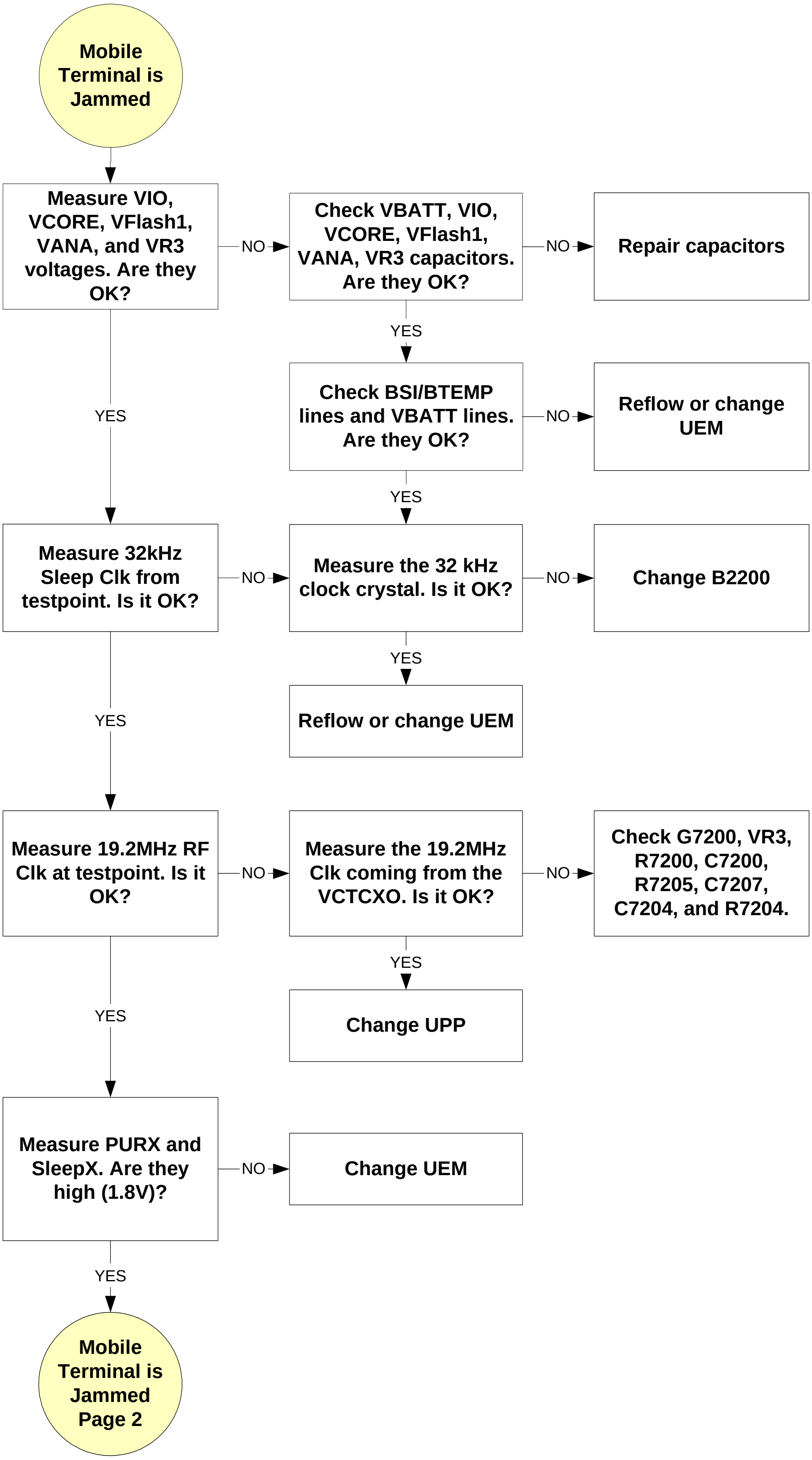


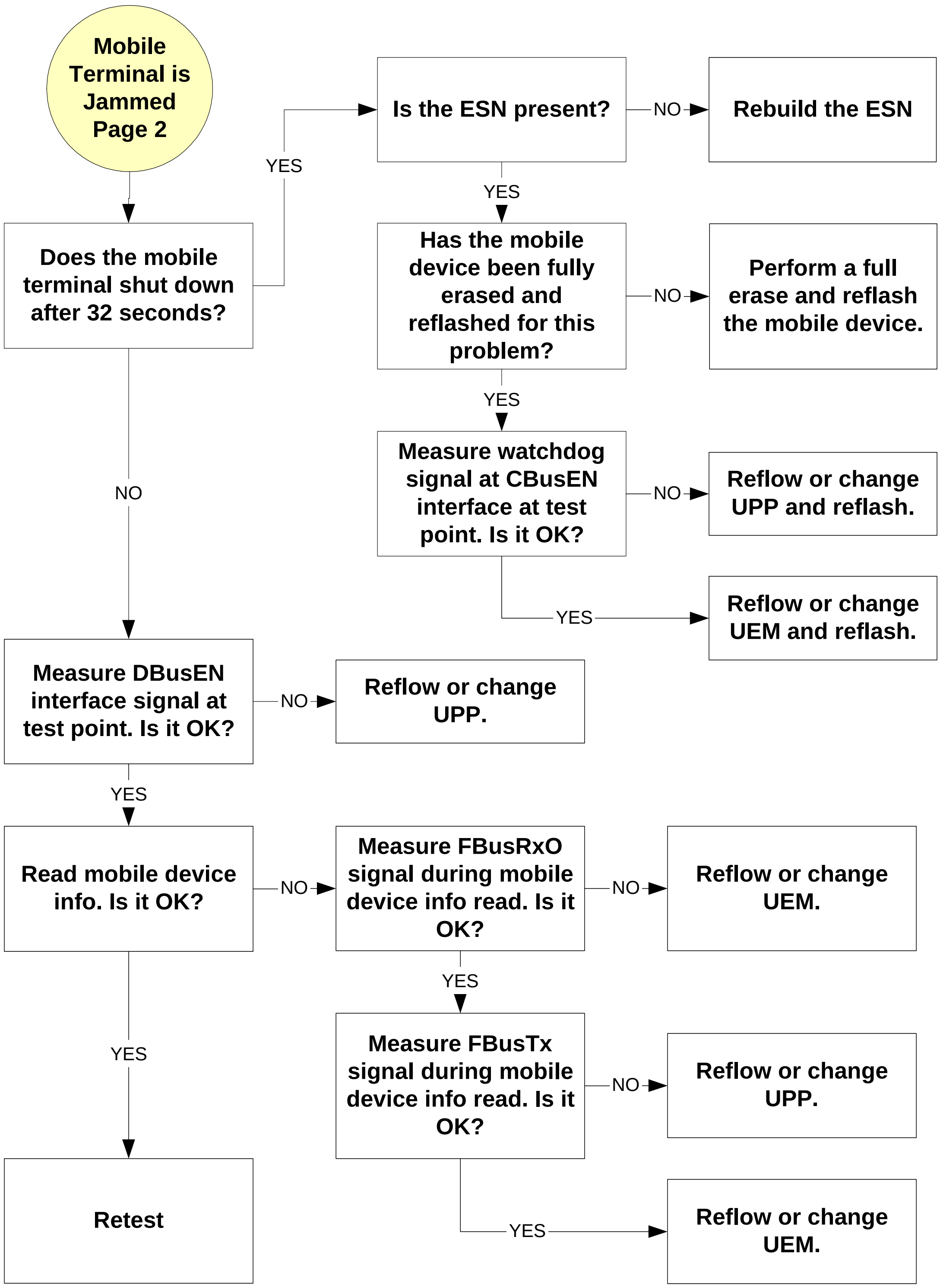
Flash Faults



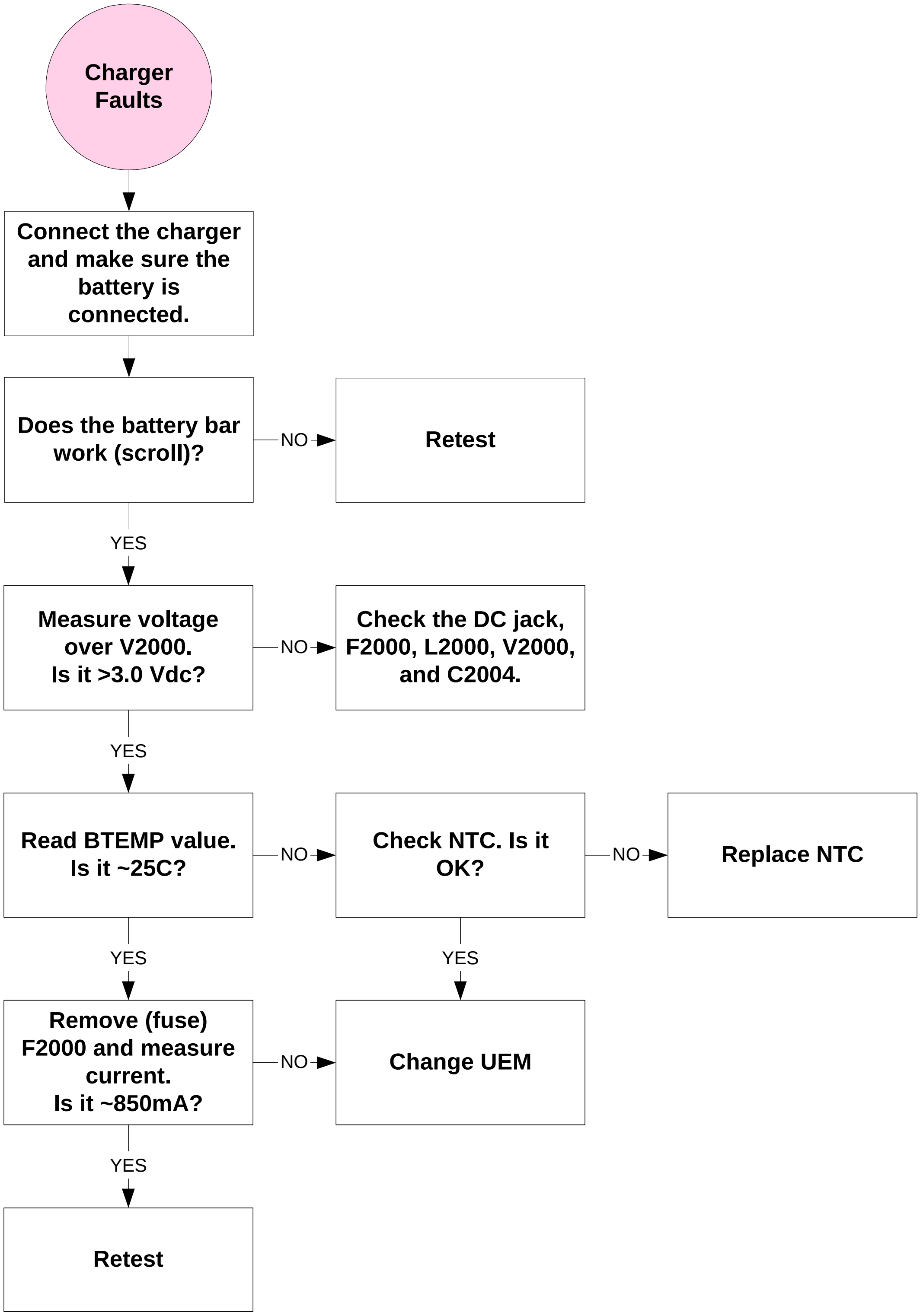

Flash Faults Page 2
Can you read the manufacturer ID and the device ID?
NO
Re-flow or change the Flash.
YES
Is the mobile terminal totally dead?
YES
Mobile Terminal is Dead
NO
Does the mobile terminal not start up or appear jammed?
YES
Mobile Terminal is Jammed
No
Retest

Power Does Not Stay on or the Mobile Terminal is Jammed

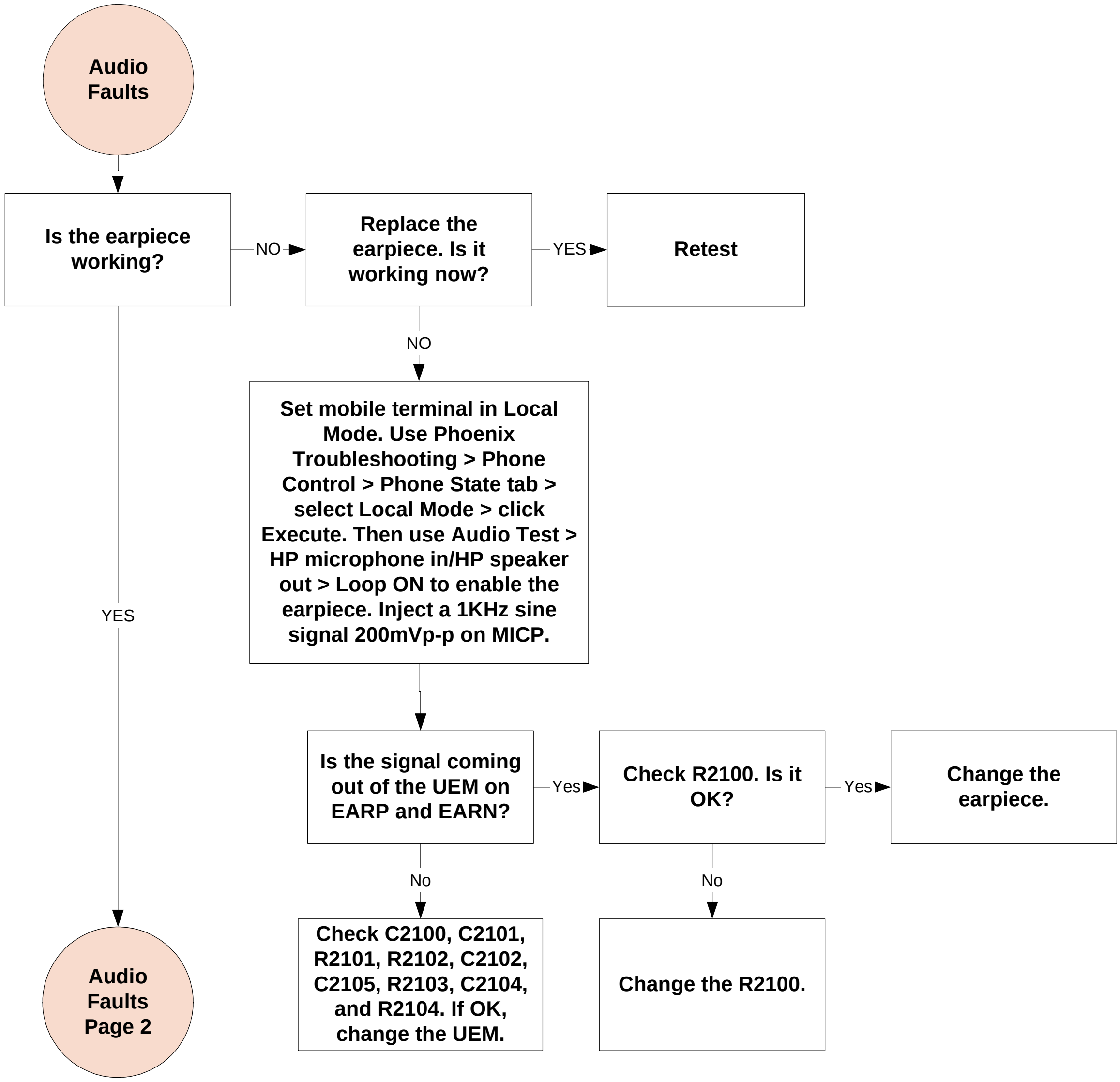


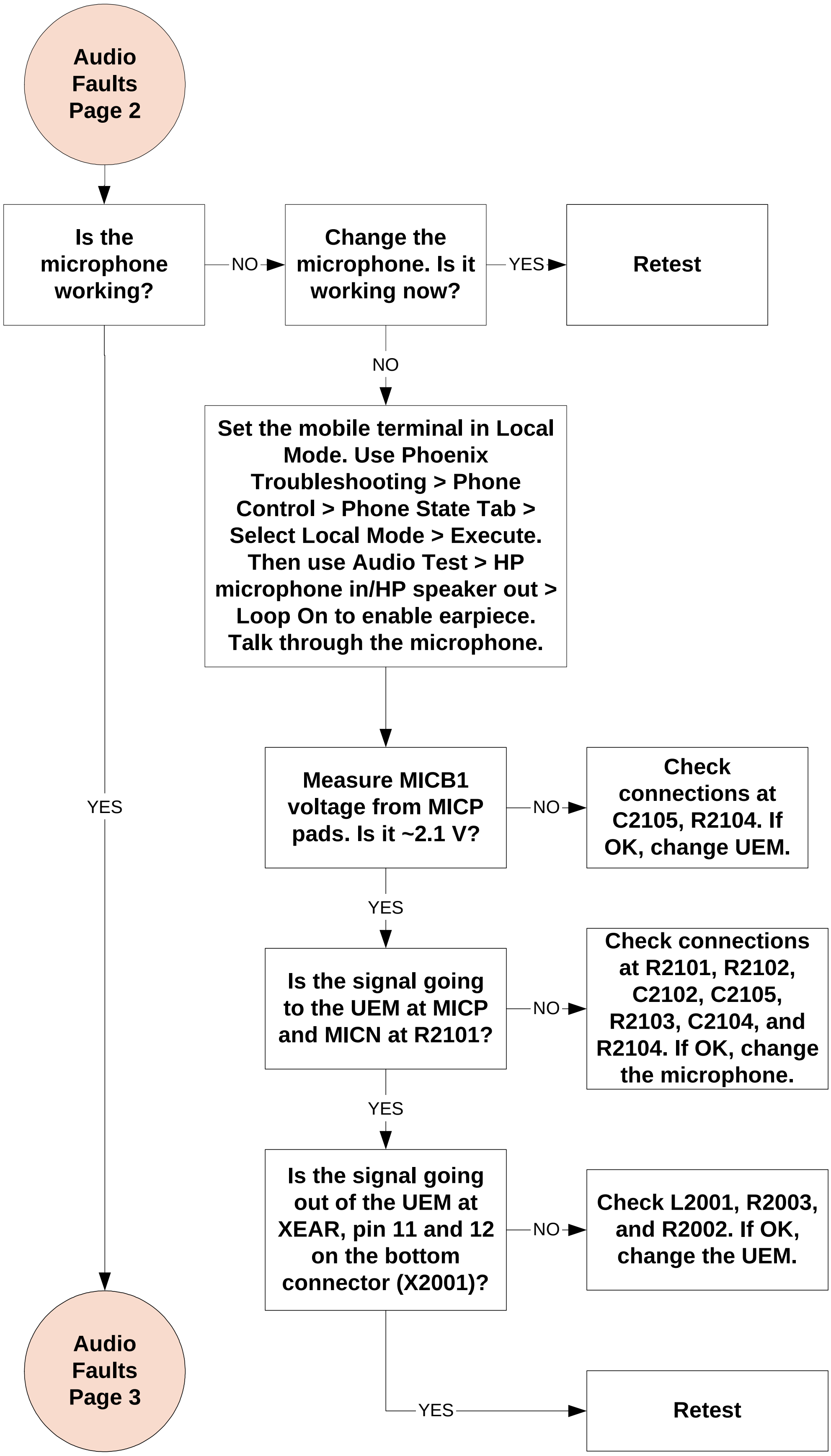

Mobile Terminal is Jammed Page 2
Does the mobile terminal shut down after 32 seconds?
YES
Is the ESN present?
NO
Rebuild the ESN
YES
Has the mobile device been fully erased and reflashed for this problem?
NO
Perform a full erase and reflash the mobile device.
YES
Measure watchdog signal at CBusEN interface at test point. Is it OK?
NO
Reflow or change UPP and reflash.
YES
Reflow or change UEM and reflash.
NO
Measure DBusEN interface signal at test point. Is it OK?
NO
Reflow or change UPP.
YES
Read mobile device info. Is it OK?
NO
Measure FBusRxO signal during mobile device info read. Is it OK?
NO
Reflow or change UEM.
YES
Measure FBusTx signal during mobile device info read. Is it OK?
NO
Reflow or change UPP.
YES
Reflow or change UEM.
YES
Retest

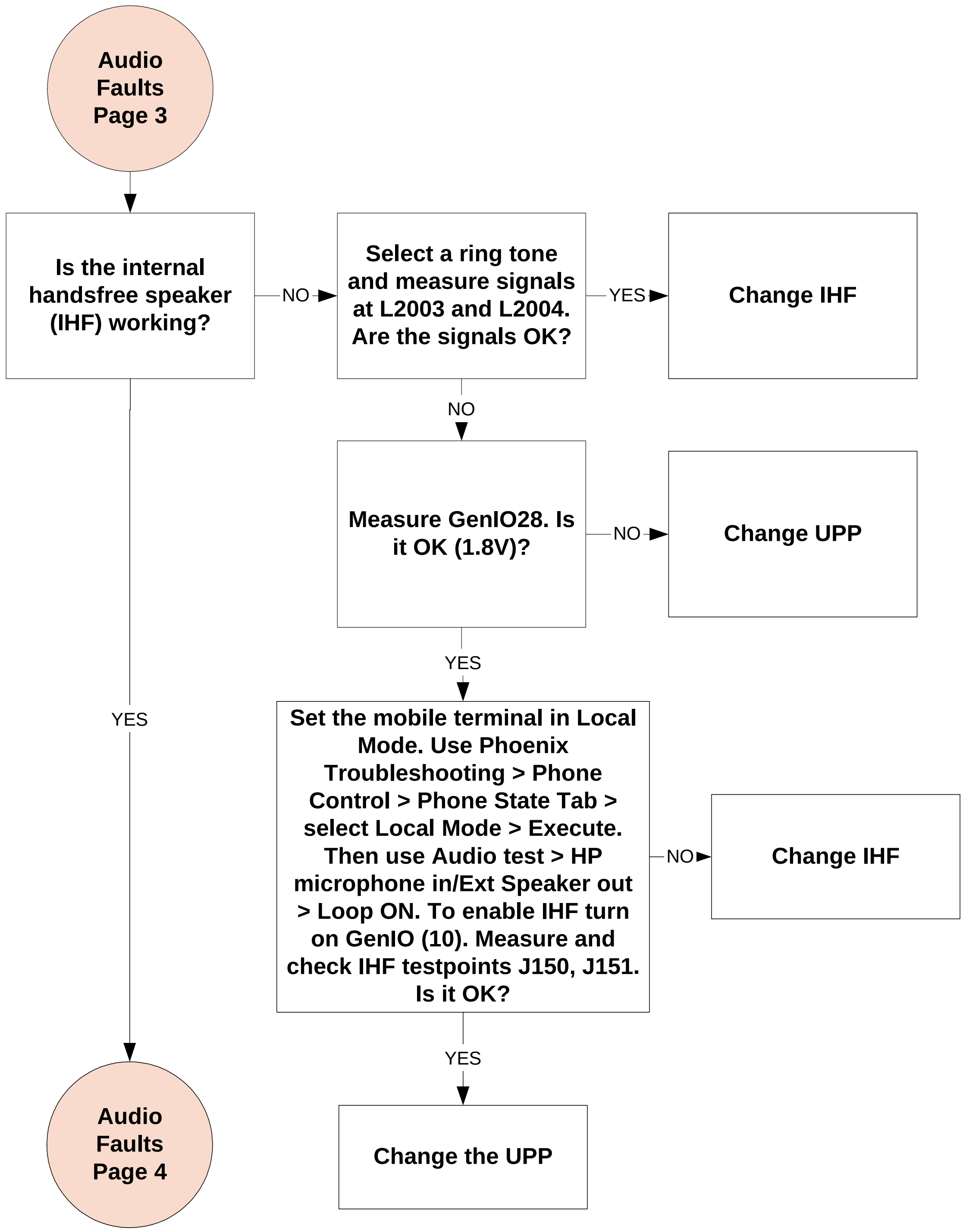
Charger Faults

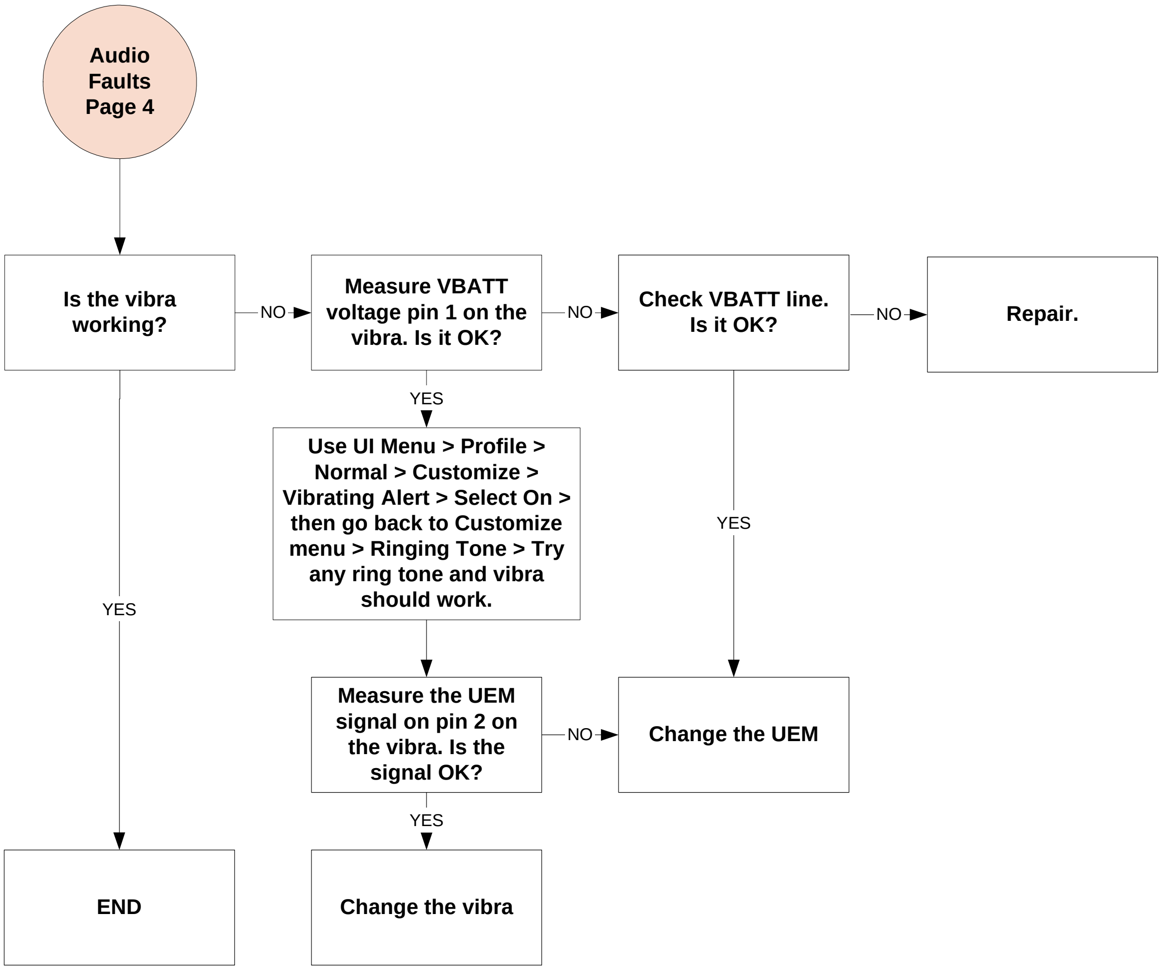


Audio Faults

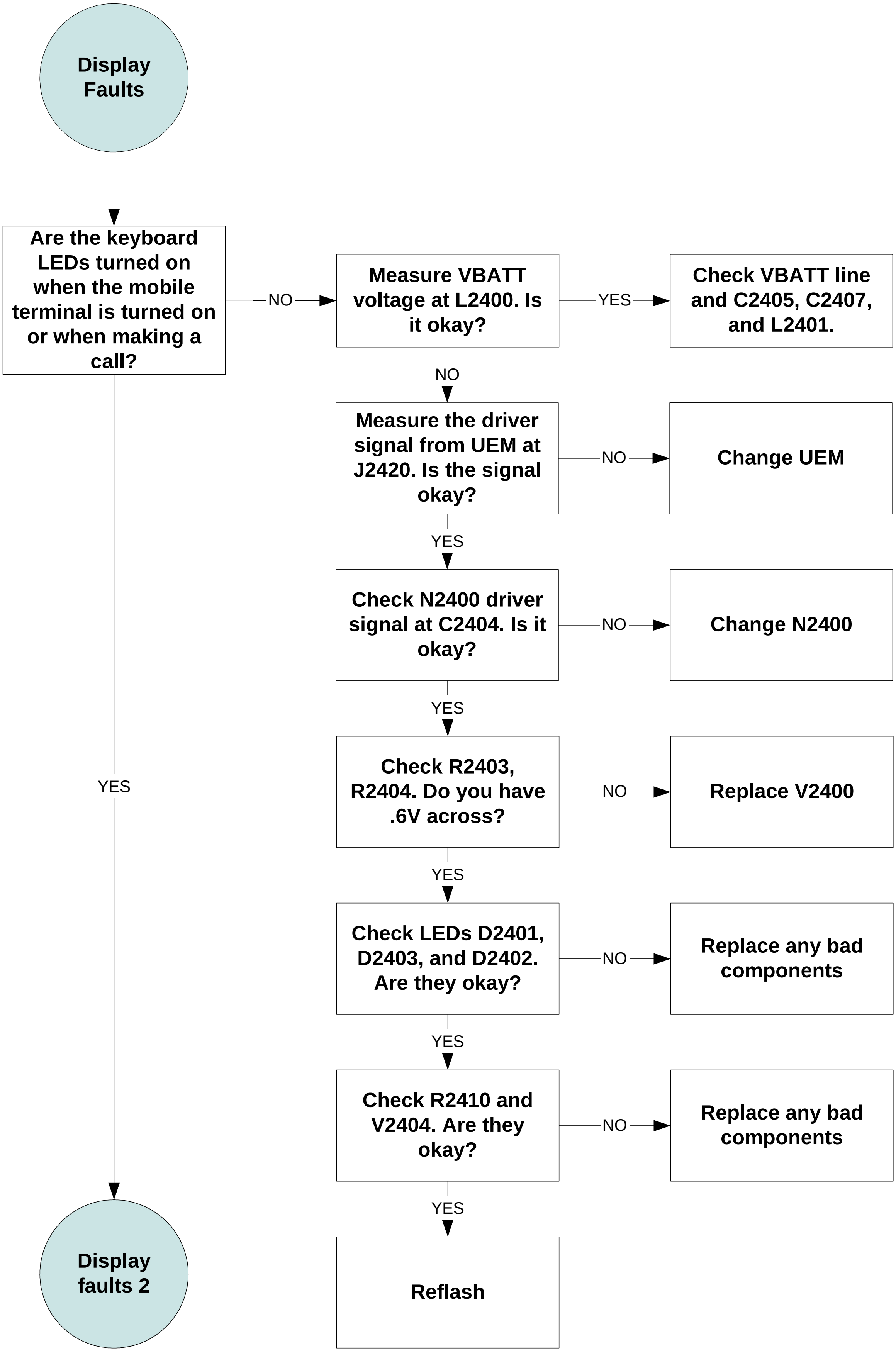


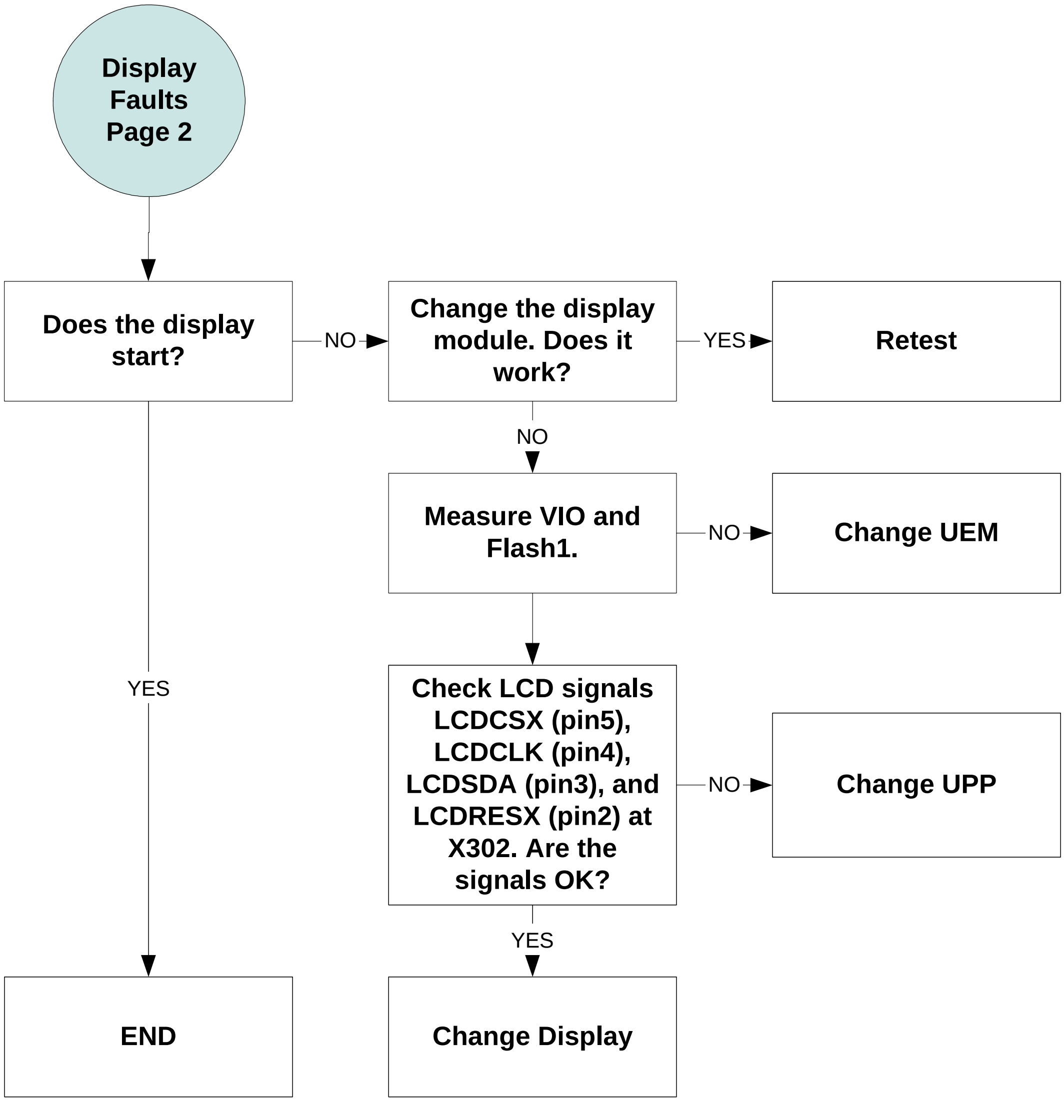

Audio Faults Page 2
Is the microphone working?
NO
Change the microphone. Is it working now?
YES
Retest
NO
Set the mobile terminal in Local Mode. Use Phoenix Troubleshooting > Phone Control > Phone State Tab > Select Local Mode > Execute. Then use Audio Test > HP microphone in/HP speaker out > Loop On to enable earpiece. Talk through the microphone.
Measure MICB1 voltage from MICP pads. Is it ~2.1 V?
NO
Check connections at C2105, R2104. If OK, change UEM.
YES
Is the signal going to the UEM at MICP and MICN at R2101?
NO
Check connections at R2101, R2102, C2102, C2105, R2103, C2104, and R2104. If OK, change the microphone.
YES
Is the signal going out of the UEM at XEAR, pin 11 and 12 on the bottom connector (X2001)?
NO
Check L2001, R2003, and R2002. If OK, change the UEM.
YES
Retest
YES
Audio Faults Page 3


Audio Faults Page 3
Is the internal handsfree speaker (IHF) working?
NO
Select a ring tone and measure signals at L2003 and L2004. Are the signals OK?
YES
Change IHF
NO
Measure GenIO28. Is it OK (1.8V)?
NO
Change UPP
YES
YES
Set the mobile terminal in Local Mode. Use Phoenix Troubleshooting > Phone Control > Phone State Tab > select Local Mode > Execute. Then use Audio test > HP microphone in/Ext Speaker out > Loop ON. To enable IHF turn on GenIO (10). Measure and check IHF testpoints J150, J151. Is it OK?
NO
Change IHF
YES
Audio Faults Page 4
Change the UPP

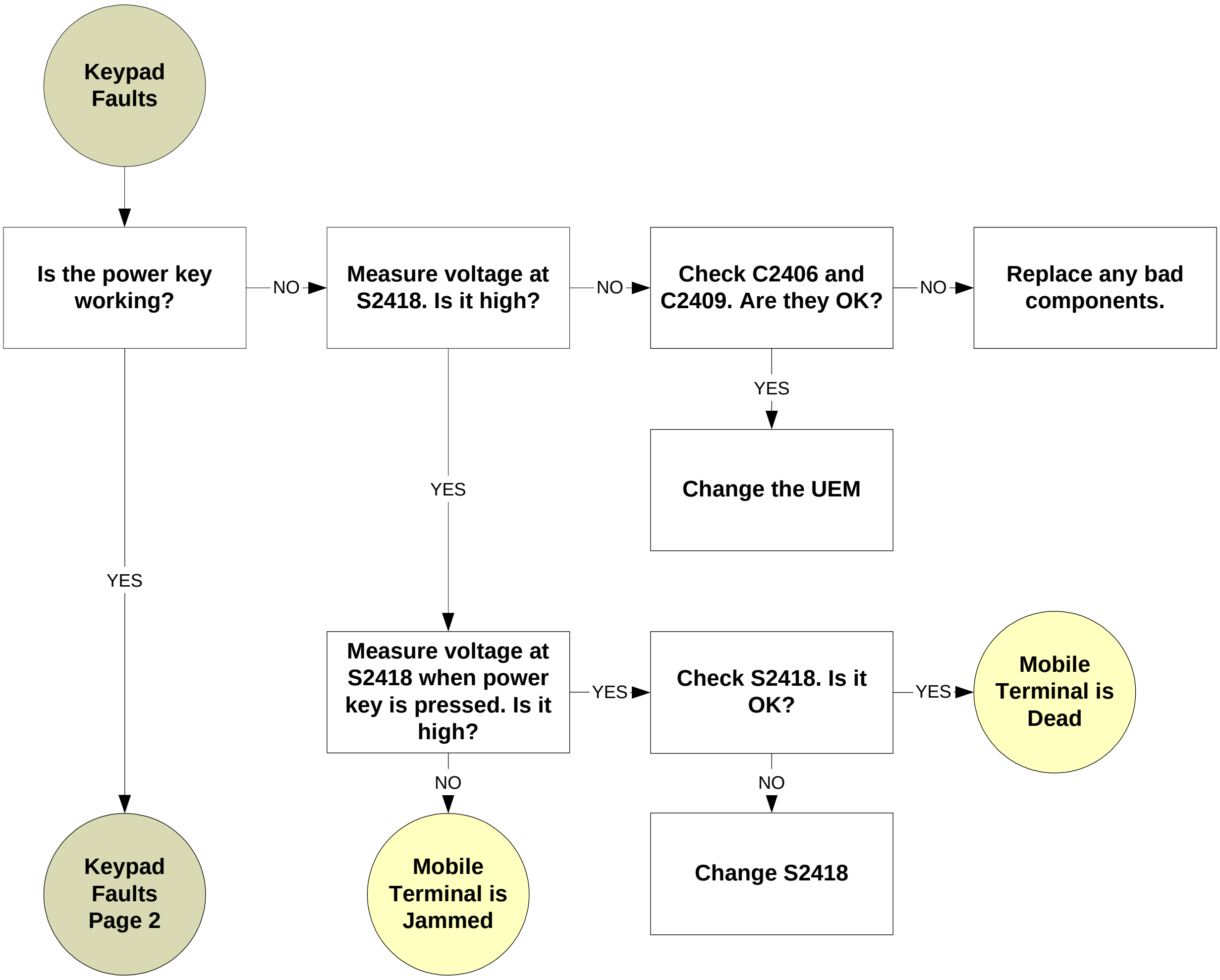

Audio Faults Page 4
Is the vibra working?
NO
Measure VBATT voltage pin 1 on the vibra. Is it OK?
NO
Check VBATT line. Is it OK?
NO
Repair.
YES
Use UI Menu > Profile > Normal > Customize > Vibrating Alert > Select On > then go back to Customize menu > Ringing Tone > Try any ring tone and vibra should work.
YES
YES
Measure the UEM signal on pin 2 on the vibra. Is the signal OK?
NO
Change the UEM
YES
END
Change the vibra

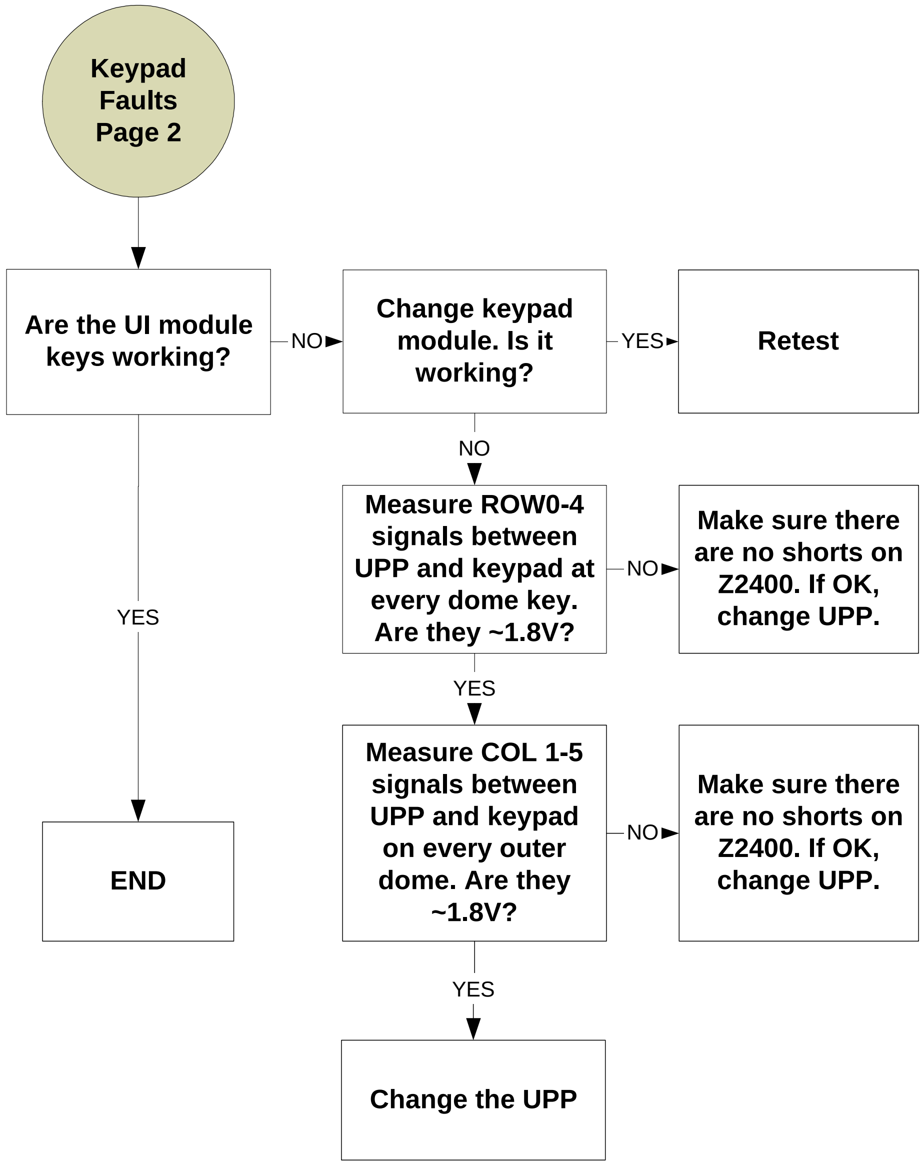
Display Faults



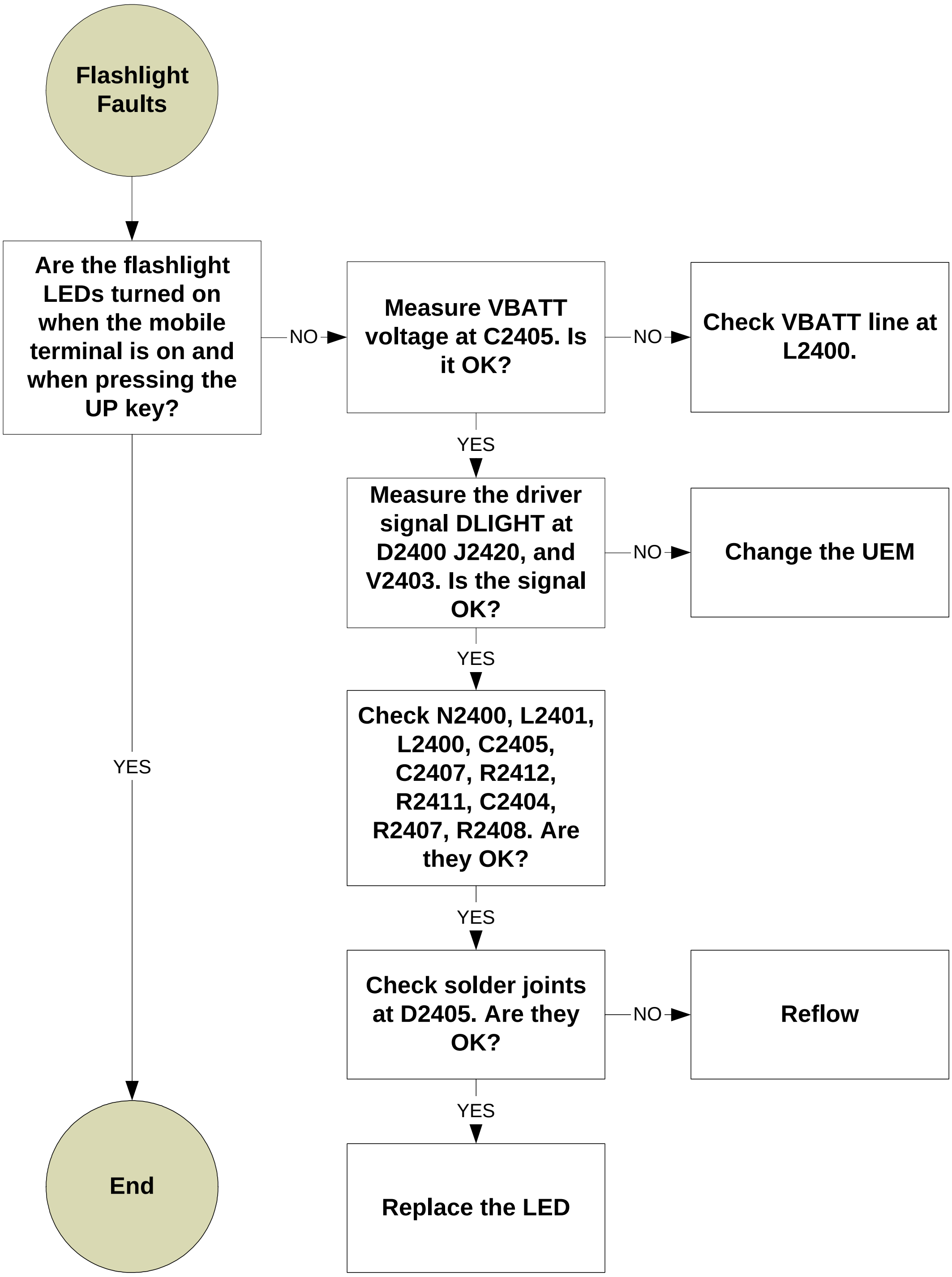

Display Faults Page 2
Does the display start?
NO
Change the display module. Does it work?
YES
Retest
NO
Measure VIO and Flash1.
NO
Change UEM
YES
Check LCD signals LCDCSX (pin5), LCDCLK (pin4), LCDSDA (pin3), and LCDRESX (pin2) at X302. Are the signals OK?
NO
Change UPP
YES
END
Change Display

Keypad Faults

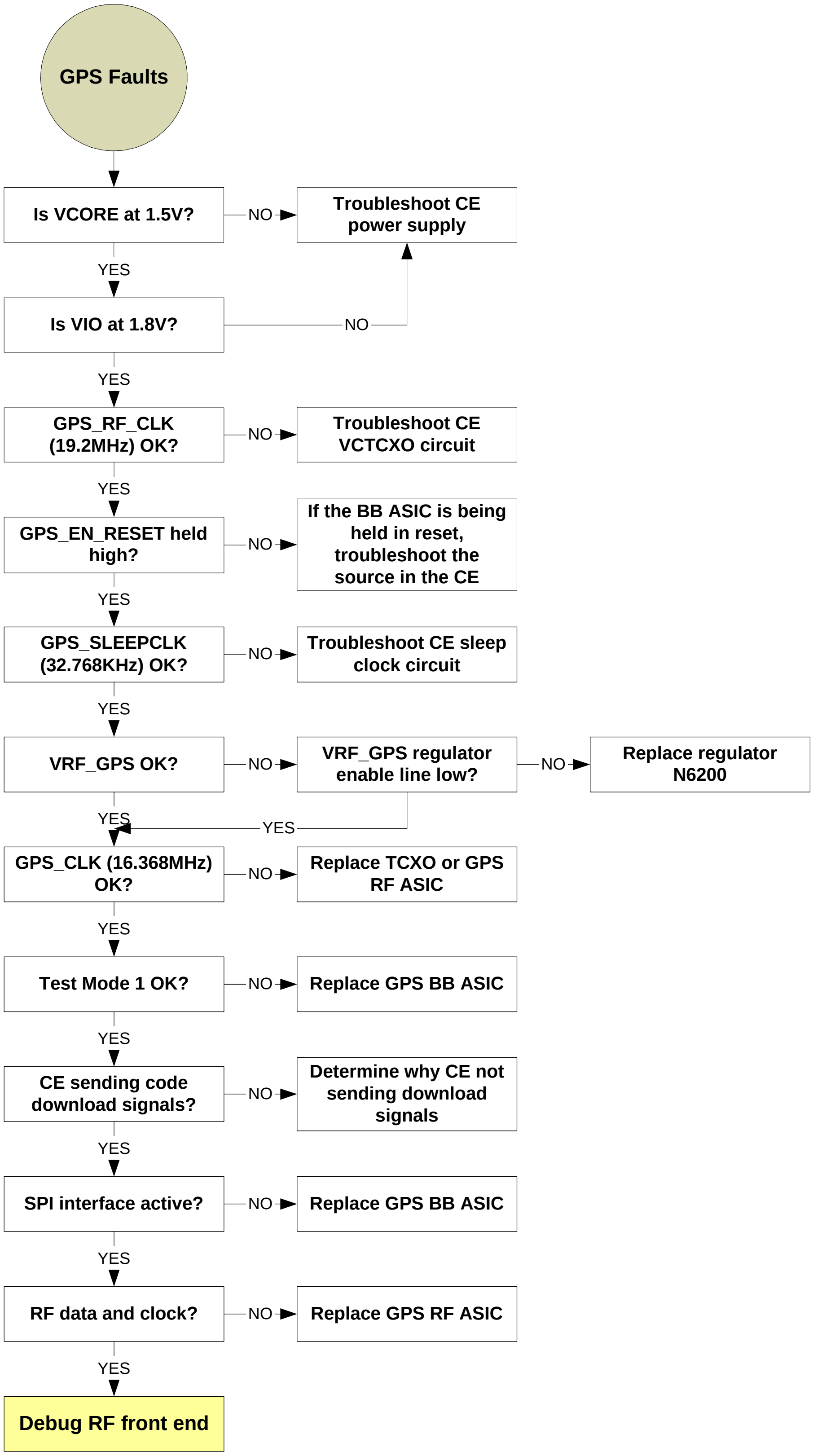



Keypad Faults Page 2
Are the UI module keys working?
NO
Change keypad module. Is it working?
YES
Retest
NO
Measure ROW0-4 signals between UPP and keypad at every dome key. Are they ~1.8V?
NO
Make sure there are no shorts on Z2400. If OK, change UPP.
YES
Measure COL 1-5 signals between UPP and keypad on every outer dome. Are they ~1.8V?
NO
Make sure there are no shorts on Z2400. If OK, change UPP.
YES
Change the UPP
YES
END

Flashlight Faults



GPS Faults


GPS Faults
Is VCORE at 1.5V?
NO
Troubleshoot CE power supply
YES
Is VIO at 1.8V?
NO
YES
GPS_RF_CLK (19.2MHz) OK?
NO
Troubleshoot CE VCTCXO circuit
YES
GPS_EN_RESET held high?
NO
If the BB ASIC is being held in reset, troubleshoot the source in the CE
YES
GPS_SLEEPCLK (32.768KHz) OK?
NO
Troubleshoot CE sleep clock circuit
YES
VRF_GPS OK?
NO
VRF_GPS regulator enable line low?
NO
Replace regulator N6200
YES
YES
GPS_CLK (16.368MHz) OK?
NO
Replace TCXO or GPS RF ASIC
YES
Test Mode 1 OK?
NO
Replace GPS BB ASIC
YES
CE sending code download signals?
NO
Determine why CE not sending download signals
YES
SPI interface active?
NO
Replace GPS BB ASIC
YES
RF data and clock?
NO
Replace GPS RF ASIC
YES
Debug RF front end

